10 Years Production Using the GaAs MESFET DIOM Process

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1. Introduction

Since 1975 Siemens has been engaged in research and development of III/V semiconductor components and circuits. The world's first commercially available GaAs MMIC was created by Siemens in 1981. Continuous activities include development of materials, processes, models and circuits on the basis of MESFET, HEMT and HBT active devices. Siemens has successfully designed and fabricated discretes and MMIC's from the MHz region up to 90Ghz operating frequency.

Besides a family of discrete devices the GaAs group has designed low noise amplifiers, driver amplifiers, power amplifiers, variable gain stages, distributed amplifiers, phase shifters, SPDT switches, mixers, broadband tuners, oscillators, and more combinations of them up to multifunction MMICs like complete receiver-, transmitter- and transceiver-circuits.

The annual production rates have been expanding in the past and are growing in the next years even more rapidly driven by the booming mobile communication market. The commercial success of the mostly SMD packaged devices is based especially on the DIOM MESFET (ref.1-4) products.

In the meantime the process is running under high volume production on 100mm wafers with more than 40k wafer starts in 1998. The next major step will be the startup of the 150mm wafer fab before year 2000.

2. Siemens DIOM Process Flow

The Siemens GaAs MESFET DIOM Process (table 1) was developed in the first half of the previous decade. This unique Siemens self aligned MESFET process was patented in 1984. The process uses ion implantation through a sputtered SiN cap layer. The later contact regions are defined in a lithography process and selectively implanted with Si and Ge. In the next step the channel area is lithographically defined and the selective Si channel is implanted. The active channel is supported by a p-buried layer implant. The process sequence requires no dry or wet etching of a mesa. The implants are annealed by RTA (Rapid Thermal Anneal). The next step is the very unique key stone of the process. In the first metal step the FET Ohmic and Schottky parts are defined in a single lithography step. Therefore the Ohmic and Schottky parts of the FET are self aligned to each other. The basic SiN layer is dry etched by a F-based RIE (Reactive Ion Etch). The first metal is deposited on the GaAs by evaporation. It is a multi layer sequence containing a highly stable W barrier. After the alloy process the active FET device is completed. This process sequence is called DIOM as an acronym for Double Implantation One Metallisation.

The benefits of this process flow are the key features: self aligned Ohmic and Schottky parts, no critical wet/dry recess etch, no wet/dry mesa etching, no metal layer crossing mesa edges, no lithography problems due to the topology of
Ohmic metal layers in the lithographic definition of the Schottky part.

All these benefits give an essential advantage in large volume production and are directly transferred to better yield performance, enhanced uniformity of electrical parameters across the wafer and from wafer to wafer.

All passive elements as needed in the MMICs are fabricated in parallel in the further wafer processing. The wafer is passivated by a double SiN layer. This layer acts as the dielectric for the MIM capacitor also. A CrNi thin film resistor is evaporated followed by second metallisation. This metal defines the capacitor top plates and the strip lines. A second passivation layer of SiN is deposited. The third metal step on the wafer front side is an Au electro-plating step. Here the current carrying capability of the metal lines are enhanced and the air bridges for low capacitance interconnects are defined.

- SiN cap layer
- selective ion implantation's
  contact area: Si, Ge
  channel area: Si, Mg
- reactive ion etch of cap layer
- joint Ohmic, Schottky metal
- evaporation (self aligned gates)
- first SiN passivation
- accurate thin film resistor
- second metal evaporation
- second SiN passivation
- plated Au air bridge interconnections
- mounting to substrate and thinning
- substrate via holes
- backside plating
- backside saw street etch
- 100% testing and dicing
- SMD packaging

Table 1: Wafer Process Flow

The backside processing of the wafers starts with a wax bonding of the wafers to a glass substrate. The wafers are thinned down to 150μm or if substrate via holes are required down to 95μm. The via holes are wet etched and the backside metal is deposited, followed by plating the Au heatsink for high power devices. After demount and final testing the wafers are sawn and the chips are assembled into mostly SMD packages.

3. Wafer Fabrication and Equipment

The production experience for GaAs wafer production has started already in the early 80's. With the transfer to 3" wafers in 1988 and the installation of i-line stepper technology semiautomatic tracks with cassette to cassette features were introduced. Reduction of particle count and the defect density and the step from contact printers to stepper lithography resulted in a yield increase by more than 25%.

Basic requirements for high volume production besides a robust process are continuous training of operator personnel, skilled maintenance groups together with a consequent maintaining schedule and statistical process control (SPC) throughout the line.

The production equipment used in the Siemens line is dedicated to volume production and the equipment selection is oriented to the Si main stream equipment road map. The SiN layers are deposited in Perkin-Elmer sputtering tools. The process speed is enhanced using magnetron assisted sputtering. The SiN passivation layers are deposited in plasma CVD tools like Applied Materials P5000. For very special features a photo assisted process is also available.

Dry etching of SiN layers is performed in parallel plate or RIE modes on Tegal, LAM or TePla systems. The well known CF₄, CF₄/O₂, SF₆ chemistries are applied.

For the sensitive ion implantations tools from Varian EH500P, Applied Material P19000, Eaton NV6200 are used. Highly preferable are systems with high mass resolution for the implantation of ²⁸Si implantation of ²⁸Si is not recommended because of possible co-implantations with N₂ or CO etc.

The lithography process is run with standard Si fab used resist spinners and developers from e.g. DaiNippon or CONVAC. AZ type photo resists are used for all lithography steps. The i-line steppers from ASML are used with NA of 0.4 and 0.6. The mask are fabricated in house on the same fab site with the advantage of shortest cycle times. For the metal layer lithographies the image
reversal mode of the AZ resist is used. This allows a lift-off process after metallisation.
The metals (Cr, CrNi, Au, Ti, W, Pt) are deposited in an electron beam evaporation technique using Temescal equipment in an orthogonal or aperture (planetary) configuration. The lift off is performed on fully automatic cassette to cassette systems using NMP as a resist solvent.
Before starting the backside process the wafers are mounted to substrates. Thereafter they are thinned down to 95μm. The backside resist processes are manufactured on the same equipment as used in the frontside process. The illumination is performed on contact / proximity printers using the infrared through the wafer technique or backside to frontside aligners.
The via holes are wet etched using a phosphoric based etch on a standard DanNippon cassette to cassette spray etching system.
The inline process control is performed on PCM structures dedicated to specific processes. The electrical testing is done with Electroglas automatic cassette to cassette probers and Rheedholm electrical test systems. Fully automatic cassette to cassette RF PCM testing is also applied in the line.

4. Products

The product spectrum of the DIOM MESFET discretes and MMICs is competitive on a global scale as demonstrated by the following examples.

For the mobile communication market in the frequency range from 900MHz up to 2500MHz a variety of devices are available covering the complete spectrum from low noise, buffer amplifier, mixer, switches to the domain of power FET’s and MMICs.
Low noise amplifier like CGY60 and CGY59 deliver 13 dB gain associated with a NF<1.6dB @900MHz. Further benefit is the high backward isolation of 25dB, making the device well suited as buffer amplifier or gain block. Supply voltage is only 3V and the package is an MW6 (a derivative of SOT143). Further devices like CFY30 and CFY35 low noise discrete FET complete the input rail. Mixer MMICs like CMY210 deliver ultra linear performance with a very high IP3in of typ. 25dBm. The low LO power requirement of 0 dBm wide LO application range from 0.5 to 2.5GHz are achieved at a low DC current of < 6mA @3V supply. The 3rd order IMD of typ. 56 dBc is a further outstanding feature. This device is very attractive for the CDMA and TDMA systems with their high linearity specifications.
The spectrum of devices required in the input regime of mobile handsets is furthermore supported by the Siemens Si-Bipolar IC’s and discrete device families generating their outstanding performance out of a process with fT=25GHz.
The transmitter part of mobile systems have different output power and gain requirements dependent on the system. In any case this part shows the highest power consumption and as a result the PAE and low 3V supply are of major importance. The discrete power FET family CLY2,5,10,15 with gate width in the range from 2 to 16 mm deliver Pout up to 33 dBm. Very high efficiencies of up to 65% are achieved. The devices are assembled in standard or modified SOT223 SMD plastic packages. The powerFET’s are supported in the line up chain by Si-Bipolar devices or variable gain amplifier like CGY120 and CGY121. These MMICs show gain control ranges of >50dB for GSM, PCN and other applications. They are available in MW6 packages.

![DECT MMIC Chip CGY195](image)

The next device family covers the broad field of power amplifier MMICs dedicated to the specific systems like DECT, GSM, PCN, PCS, etc. A few examples out of the production portfolio are highlighted. Broadband amplifier 0.8GHz to 3GHz like CGY195 have single supply voltage only in the range from 2.7V to 6V. With a Pout of 26dBm at 3V and an overall PAE of up to 50% this 3 stage device is best suited for DECT (fig.1). The package is a small SCT595. For the PCN/PCS systems a power level of Pout=31.5 dB is required. The devices like CGY181 support the
system at 3.6V with 37% PAE. Package in this case is 12 pin derivative of the SOT223 package. Power amplifier MMICs for GSM class 4 phones require Pout of typ. 35dBm at the MMIC level. This is realized in the CGY96 a fully integrated 3 stage amplifier with single supply operation (fig.2). The negative voltage required by the internal control circuit is generated on chip. The power control circuit covers a dynamic range of 80dB. The overall PAE of 50% is achieved. The device is delivered in a 16 pin plastic package with integrated heat slug. Further DAMPS and TDMA systems are supported by CGY81 and CGY191. The upcoming dual band systems CDMA/AMPS/TDMA or GSM/PCN are addressed with the devices CGY0819 and CGY0918.

Figure 2: GSM MMIC Chip CGY96

Application examples outside mobile com are L-band tuners, K-band radio links, further military and space applications like S-, C- and X-band phased array radar (PAR) chip sets. These active antenna chip sets contain the electrical functions LNA (low noise amplifier), PHS (digital controlled phase shifter), VGA (digital controlled variable gain amplifier) and HPA (high power amplifier). In dual chip assemblies 11 Watt were realized in S-band, based on 6 Watt MMICs. For the COBRA C-band phased array antenna the complete chip set has been delivered for the engineering antennas already in 1993. In the present pre production phase 3 stage MMICs have been manufactured with Pout=8Watt and PAE of up to 40%. Multi function chips (ref.4) delivering small signal functions together with medium power amplifier like in MLS (5bit PHS, 6 bit VGA and medium power Amp.) are realized on a single chip (fig.3). Further developments are 2 stage amplifier in X-band. Output power levels of 7 Watt with PAE of 35% have been realised and 10 Watt are targeted in the current run.

5. Quality Assurance

The quality assurance for the Siemens GaAs production is completely embedded in the Siemens semiconductor quality system. The TQM (Total Quality Management) philosophy targets the work towards total customer satisfaction with defined corporate objectives. The GaAs wafer line is qualified to internal and external standards (QS 9000). Quality assurance for GaAs products is applied throughout the complete production chain. Processes and equipment are under SPC (Statistical Process Control). The quality of the products is checked by various standard process controls on wafer and comprising DC test at different fabrication steps. For assembled products a general production release is
mandatory including over-stress tests HTB (High Temperature Burn-In), HTRB (High Temperature Reverse Bias), IOL (Intermittent Operating Life), thermal sequences and additional environmental tests). After the initial release, a periodic reliability monitor ensures the high quality level of the devices by performing over-stress tests at regular intervals on products from the process families.

In 1997 the Power MESFET CLY32 as a representative of the DIOM power MESFET family was formally space qualified according to ESA/SCC qualification procedures. The Siemens discrete HEMTs (deviating from the DIOM FETs in substrate material, MBE layers and gate module, but having identical passivation schemes and interconnection techniques including air bridge technique and backside processing) have already been ESA/SCC space qualified in 1994 (ref.5).

6. Conclusion

The process capability of the Siemens DIOM line covers the complete domain of analog MESFET applications. The quality and reliability are outstanding as demonstrated by the space qualification of the power MESFET. The process has been proven over more than 10 years as a manufacturable process suitable for high volume wafer production.

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