ELECTROCHEMICAL ETCHING IMPACT ON GaAs PROCESS, MASK DESIGN AND DEVICE PERFORMANCE

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Abstract

An enhanced consumption of the GaAs material is observed in the vicinity of metal structures exposed during wet processes. It has a pronounced impact on the electrical performance of the fabricated device, and may be observed visually. The damage occurs whenever a wet processing, either cleaning\oxide removal or etching is performed. The effect on electrical parameters and visual appearance and its magnitude depends on process conditions and the chemistry involved. This paper presents electrical measurements and observations of the possible damage to the device and suggests different approaches to reduce this effect.

INTRODUCTION

GaAs etching rate and shape in a given solution can be altered by the presence of a metal substance on the GaAs substrate surface due to the Galvanic effect[1]. This so-called electrochemical effect is the result of the electric circuit formed between the semiconductor, acting as an anode, and the metal as a cathode. The circuit is shorted by the etchant solution on one side and the semiconductor material or conducting epitaxial layers on the other. It was suggested[2] that this effect be used to control the threshold voltage of GaAs MESFETs by varying the size of metal pattern exposed to the solution during the gate recess process step. Another suggestion[3] was to use metal-exposed pattern during InAlAs/InGaAs heterojunction field effect transistors (HFET) processing to change etching characteristics in short gate length recesses.

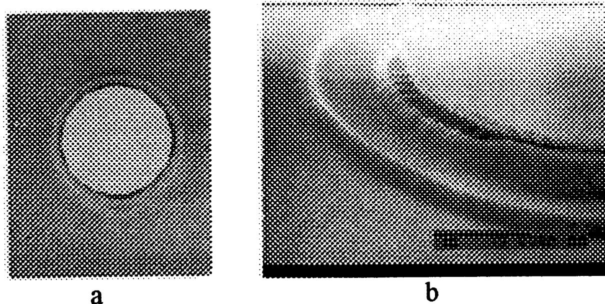
However, in some processes this galvanic effect is accompanied by unintentional etching of the semiconductor material resulting with poor definition of the device, pits and holes on its surface, disconnection and bad contacts between GaAs and metal layers.

In the present work we investigated the effect of such etching on device production and performance from two aspects:

1. The lateral etching in the vicinity of metal substance on top of mesa structures. The mesa etching processes are used to isolate masked areas from one another to avoid short circuiting the fabricated devices via conducting layers. This etching may extend up to a few microns in depth. It is common to assume that lateral and perpendicular etch rates are about the same with no metal present in the solution when etching process takes place.
2. Another unintentional etching process of the GaAs material takes place during various wet surface treatments on the entire, unmasked wafer. These treatments are performed to provide fixed surface conditions for better control and reproducibility of the process, and to remove native oxide layers that may have formed on the wafer surface. These treatments include rinsing with DI water, which was found to react as an etchant too[4].

EXPERIMENTAL

The first undesired etching effect described below examined the use of phosphoric acid based etchant[5] with SiN mask for mesa etching. Fig 1a shows a metal pattern on the top of a deep mesa. This is a typical picture for in-line visual inspection by metallurgical microscope. No significant undercut of lateral etching may be observed from the top view. However, a detailed side vie inspection by SEM shows pronounced undercut, due to the enhancement of the etch rate in the vicinity of the exposed edges of the metal (Fig1b).



a b

Fig 1.a.-Top view of the metal pattern with SiN mask on top of deep mesa. b-SEM Side view of the pattern shown in Fig 1a. (Metal with two steps mesa etching)

It can be seen that once the metal surface is exposed the etch rate is locally enhanced (by an order of magnitude), resulting in undercuts underneath the metal layer. This undercut may not be properly detected from top view. This phenomena is avoided by changing the bias in the mesa etching mask (Fig 2.) i.e. photoresist should cover the metal with margin of at least the expected etch depth (assuming lateral etch rate equals perpendicular etch rate with no metal present in the solution).

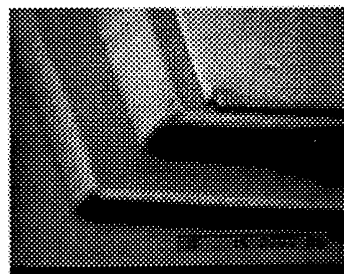


Fig 2. Properly biased pattern. (Metal with two steps mesa etching) No electrochemical etching is observed

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Another approach to the problem is to change the whole process flow (if possible) so that all deep mesa etching steps are performed before any metallization is applied to the wafer.

In the second loop of experiments an epitaxial wafer after ohmic contacts metal definition was cleaved to pieces.

Each piece passed a number of oxide removal surface treatments (that simulate the number of treatments performed in the manufacturing process of a device), in different alkaline or acidic solutions.

This experiment also examines if metal alloying process has an effect on the galvanic cell potential formed in the vicinity of the metal. For this purpose some of the wafers have passed thermal process in order to form alloyed contacts and others remain non-alloyed. Both sets of samples have passed the same wet treatments. The non-alloyed samples have passed the thermal process after the wet treatments in order to measure the current and sheet resistance (Rsh) in the same conditions.

These experiments were monitored by measurements of the saturation current (Idss) between two Ohmic contacts in a given structure (in a curve tracer), sheet resistance (Rsh) and visual inspections in SEM.

Table 1 describes the

TABLE 1
DIFFERENT SURFACE TREATMENTS (CLEAN/OXIDE REMOVAL) VS. SATURATION CURRENT

	Average Idss (A/mm)			
Solution/ No. Of clean	A	B	C	D
Before clean/ surface treatment	1.5	1.44	1.50	1.50
First clean	1.5	1.42	1.44	1.38
Second clean	1.5	1.40	1.36	0.65
Third clean	1.48	1.36	0.92	-

Solution A- DI water
Solution B- Dilute HCl
Solution C- Dilute ammonium hydroxide
Solution D- Dilute buffered HF

A decrease in the device saturation current can be observed whenever a surface treatment is applied, while the magnitude of the effect depends on the chemical composition of the solution. Figure 3 shows the enhanced consumption of the GaAs in the vicinity of the alloyed stack metal.

Table 1 shows a high sensitivity to chemical composition of the solution, so if a surface treatment of oxide removal (in the presence metal substance) is necessary the use of dilute HCl solution is preferable because it yields with the smallest damage.

The experiments also indicate that long rinses with DI water (around 15 min) may also reduce the current, in the same region, from 1.5 A/mm to 1.28 A/mm.

Solution C was chosen for the investigation of the effect of alloyed and non-alloyed metal on the increased consumption of the GaAs. Table 2 shows the current and Rsh figures of wafers treated with dilute ammonium hydroxide solution three times.

TABLE 2.
SATURATION CURRENT AND Rsh OF DEVICES WITH ALLOYED AND NON-ALLOYED METAL STRUCTURES

Measurement type	Alloyed	Non alloyed
Rsh (Ohm) before clean steps	151	151
Rsh (Ohm) after clean steps	159	168
Current (A/mm) before clean steps	1.5	1.5
Current(A/mm) after clean steps	0.65	0.65

The result show that the damage to the device on the wafers with the non-alloyed stack metal is of the same magnitude as in the wafers with the alloyed metal. The Rsh results imply that the damage is even larger in the vicinity of the non-alloyed stack metal. This outcome may be explained by a smaller potential difference (of the galvanic cell) between the GaAs and the alloyed metal than the one with non-alloyed metal.

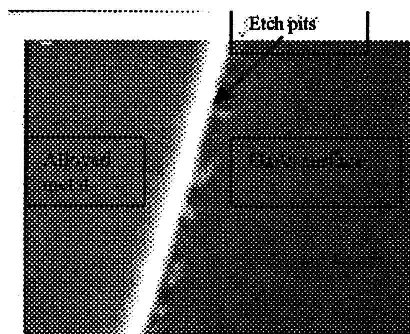

Fig3: etching pits after 2 cycles of surface treatment with dilute BHF

CONCLUSIONS

When a metal substance (alloyed or non-alloyed) is exposed (not masked) during GaAs wet processes (etching or cleaning), an enhanced consumption of the GaAs is observed in the vicinity of those structures. It has pronounced impact on the electrical performance of the device: decreasing saturation current between ohmic contacts, increasing the sheet resistance of the GaAs surface layer and the resistivity of the contacts themselves. It may even result in lifting the metal patterns off from the wafer surface. The damage to the wafer surface may be observed visually.

The experiment conclude with the following changes in process:

1. Reducing all rinse steps to minimal time and even eliminating if possible.

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2. Minimizing the number of surface treatments of oxide removal with bare metals.

3. Using, whenever possible, a surface treatment that yielded with the lowest damage to the device among all the solutions that were examined (HCl).

4. Changes were made to the mask design to take into account lateral etching in mesa etching processes, so that no metal is exposed to the solution.

5. Change steps order so that wet processes are preformed before metallization where applicable.

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