Adapting Electrostatic Chucks for Dry Etching of GaAs

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ABSTRACT

Within the silicon industry an electrostatic chuck (ESC) used with helium backside cooling has become the primary method for controlling wafer temperature during plasma etch processing. An ESC has several advantages over mechanical clamping namely: no wafer frontside contact; lower particulate levels; simpler; lower cost; higher reliability. However, when applied to GaAs (and other III-V materials), it has been found that ESCs that work well for Si can manifest a number of problems. This paper describes the adaptation of a thick dielectric capacitive ESC, widely used for Si etching in production, to GaAs processes. Methods for reducing and/or eliminating the undesirable effects seen for GaAs etching are described, along with example process results. Possible reasons for the differences between Si and GaAs processing are discussed. It also details how the thick dielectric approach allows for the processing of wafers on sapphire carriers and results for a GaAs backside etch are presented. Finally, a further adaptation of the same thick dielectric ESC technology to InP processing is presented.

INTRODUCTION

Trikon Technologies manufacture chemical vapour deposition (CVD), physical vapour deposition (PVD) and plasma etch production equipment for the semiconductor industry. CVD products include the Delta® 201, Planar® Low K Flowfill™, PVD the Sigma®, and Etch the Omega® 201. The Omega® 201 is available with a number of process chambers namely reactive ion etch (RIE), plasma-enhanced RIE (PERIE), inductively coupled plasma (ICP) and the MØRI™ helicon source, the latter two being high density plasma (HDP) sources. The Omega® 201 system is a small footprint, low cost (at least in terms of tools targeted at the silicon industry!) single chamber system with an optional downstream plasma station for anti-corrosion treatment after metal etch, and/or resist stripping. Fig. 1 shows a picture of a Omega 201 ICP system. More details on all of the above can be found on the Internet at: www.trikon.com.

All three Trikon product types offer hardware and process solutions that cover a wide range of requirements from next generation high speed silicon logic devices, to specialist applications. At one time III-V processing was considered a specialist application, at least by equipment suppliers to the

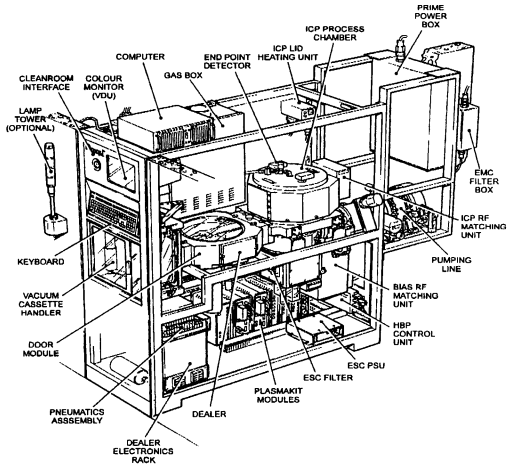


Fig. 1 Omega 201 ICP Etch System

silicon industry, but growing interest in III-V volume production has given rise to the need for production- worthy processes and equipment. i.e. reliability, repeatability, high yield, low particles, higher throughput, larger wafer size, and so on. The obvious answer was to use equipment already developed for the silicon industry and, by and large, this has proven a satisfactory solution. One area that has not transferred readily is the use of Electrostatic Chucks (ESC) in the place of mechanical clamps for wafer temperature control. ESCs now dominate in the silicon industry for reasons of cost, simplicity, particulates, and reliability. Since 1995, all Omega® 201 tools have shipped with ESCs rather than mechanical clamps, including a number of machines for III-V applications. Logically one might expect ESCs will soon displace mechanical clamps for III-Vs, but ESCs that work well for silicon can show a number of problems for III-Vs. Also III-Vs have extra requirements, e.g. backside vias in thinned wafers on sapphire carriers. To complicate matters there are a number of competing ESC technologies which it would appear will have varying degrees of success when used for III-V processes.

This paper describes the adaptation of Trikon's thick ceramic ESC to III-V processes. To aid in the understanding of this process the various ESC types are reviewed first, before looking in detail at the adaptations required for GaAs and InP processing.

ELECTROSTATIC CHUCK MECHANISMS

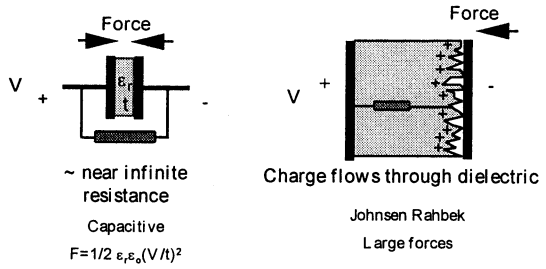


Fig. 2 Schematic of capacitive and Johnsen Rahbek clamping mechanisms.

Fig. 2 illustrates the two fundamental mechanisms by which ESCs clamp wafers. The capacitive version, based simply upon the attraction experienced between capacitor plates of opposite charge separated by a resistive dielectric is intuitive and easy to understand. The second mechanism, based on the Johnsen Rahbek (J-R) effect, is less obvious. Here, the dielectric is semiconducting so charge can leak through to the opposite capacitor plate (which is a wafer in our application). However the dielectric has an intrinsic surface roughness and a large enough resistance such that it actually generates some voltage difference between the wafer and the "valleys" of the dielectric surface. Although this voltage is small, the gaps are small enough to create large clamping forces. Because the J-R effect relies on a semiconductor effect (usually a doped alumina ceramic) there are a number of inherent difficulties to overcome:

- Precise control of the dielectric composition is required..
- It exhibits the usual temperature-dependent resistance behaviour of semiconductors. If the temperature is too low it becomes too resistive and will not clamp. If the temperature is too high it can result in high currents.
- Even in the correct temperature regime there is current flowing to, and through, the wafer.
- The clamp and declamp is dependent on charge flow to and from the wafer. Therefore it takes time for the clamping voltage to build up and dissipate.

The simple capacitive ESC does not suffer from these problems, but has the singular disadvantage of generating much smaller clamping forces than a J-R ESC.

MONOPOLAR AND BIPOLAR ESCS

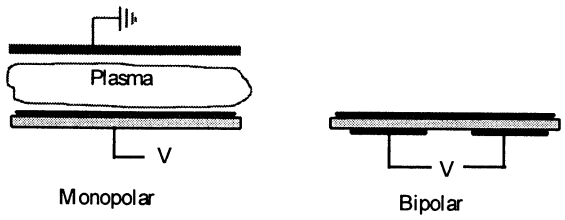


Fig. 3 Configurations for monopolar and bipolar ESCs

Fig. 3 shows two basic ways an ESC can be implemented. This applies to both capacitive and J-R ESCs. The monopolar version relies on the plasma to complete the circuit. So there is no clamping in the absence of a plasma and, even worse, a plasma will leave a dc bias on the wafer after processing which can cause problems de-chucking the wafer from the ESC. The bipolar ESC is not dependent on the plasma for clamping, and does not impose any voltages on the wafer. However a plasma can still cause dechucking problems due to residual charge and the clamping forces area quarter of those for the monopolar ESC.

THICK AND THIN DIELECTRIC ESCS

Both capacitive and Johnsen-Rahbek ESCs can be produced as thin films physically deposited onto a platen, or as thick bulk plates bonded to a platen. For a J-R ESC the conductivity of the film or plate can be adjusted to attain the optimum properties for a given thickness.. For a capacitive ESC the clamp force varies as $(V/t)^2$ where V is the applied voltage, and t the dielectric thickness. So for thin film ESCs relatively low voltages are needed, typically <1000V. For thicker ESCs larger voltages are needed, typically kilovolts. There is a fundamental choice to be made here between mechanical robustness and electrical complexity. Thin films have the drawbacks of mechanical fragility and electrical properties that are inferior to bulk , but have the advantages of:

- many established thin film growth techniques,
- good dimensional accuracy, and conformal coverage of features on a pre-machined platen (e.g. cooling grooves),
- Low voltages.

For thick plate ESCs the advantages are:

- Wide materials choice,
- bulk material quality (low leakage currents),
- mechanically robust,
- many established bonding techniques.

The biggest drawback being the high voltages, which require high voltage supplies and interconnects, which are can be looked on as safety and reliability headaches by users. Thick plate capacitive ESCs have two less obvious advantages when it comes to plasma processing.

Firstly, Fig. 4 illustrates the situation for bipolar ESCs where a plasma is imposing a DC bias of -500V onto a wafer. For a thin film ESC two problems arise because the DC bias and clamping voltages are of a similar magnitude. Firstly, for one electrode the voltages sum and impose a difference of 1000V across the film which may be beyond the breakdown voltage of the thin film material. (Note, for capacitive ESCs, the clamp forces are quite small, so the voltages are close to the dielectric breakdown voltage). Secondly, the potential across the other electrode drops to

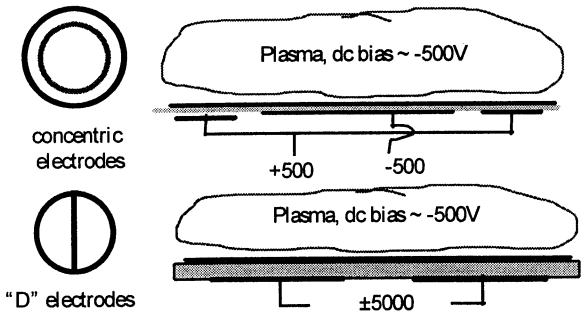


Fig. 4 ESC electrode options, top thin film, bottom thick plate.

near zero and clamping is lost. This means for a thin film capacitive ESC the electrodes must be circular, with the outer electrode always positively biased, so that the edge of the wafer is always clamped. Also a balanced power supply is needed that references the applied voltages to the dc bias, or allows the ESC voltages to float.. For a thick plate capacitive ESC, where voltages are typically an order of magnitude greater than the DC bias, these problems disappear. It is possible to use "D" electrodes and simply reference the power supply to earth. Also the polarity of the clamping voltages can be reversed between each wafer. This prevents long term charge build up and ion migration in the dielectric plate.

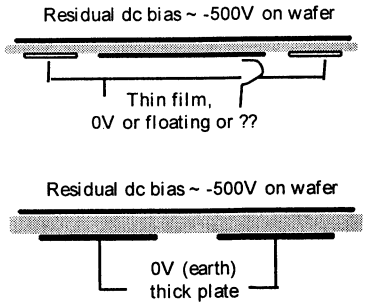


Fig. 5 Effects of residual wafer charge for thin and thick ESCs.

Secondly, Fig. 5 shows the situation for thin and thick film capacitive ESCs at the end of a process after the plasma has been turned off. In each case trapped charge remains on the wafer. Again the voltage generated is irrelevant for the thick plate ESC, but is enough to generate residual clamping for the thin film ESC, resulting in more complex de-chucking procedures. However, the thick ESC is more resistive and can prevent the residual charge leaking away, and de-chuck plasmas are sometimes required to stop the wafer "pinging" off the thick plate ESC when lifted.

Having investigated all the options, Trikon chose to pursue a thick plate capacitive ESC and deal with the problems of generating and delivering high voltages. This decision appears to have been sound, and there are now 45 Omega 201 systems world-wide running production using this ESC. By manufacturing in-house from relatively low cost materials a high degree of design flexibility is achieved, as well as a low cost (typically $8k). The ESC is guaranteed to 50,000 cycles although the typical lifetime is in excess of 500,000 wafers. The wafer overhangs the ESC edge for a few mm, there are grooves in the top surface for helium distribution, and the lift assembly is a recessed tripod in the ESC centre. This all works well for silicon, but when used for GaAs a number of problems arise.

RF COUPLING UNIFORMITY

The first thing that becomes clear when some GaAs wafers are run on an ESC developed for silicon is that there are areas where the etch rate is significantly slower. This usually only occurs for dielectric etches; for metal etches (e.g. Au sputter etch) this effect is not observed. It appears that GaAs is not always sufficiently conductive at 13.56Mhz to spread the dc bias generated by the RF across areas of the wafer which cover features on the ESC. Areas that do not etch uniformly are: those near: the wafer overhang at the edge; above the wafer lift; over a helium distribution groove; and the ESC electrode. Fig 6 shows a modified ESC configuration that deals with these problems. By using an oversize ESC it is possible to eliminate the wafer overhang, and to use an ESC electrode diameter that matches the wafer diameter. Also, by using a modified wafer lift assembly that mimics the ESC structure the RF coupling can be made uniform right across the wafer. Fig. 7 illustrates this for a dielectric film etch. The thick plate ESC is ideally suited to this application because the region outside of the wafer is RF driven and exposed to the plasma. With a thick plate of bulk material quality this exposure does very little harm, but for a more delicate thin film ESC this is unlikely to be the case.

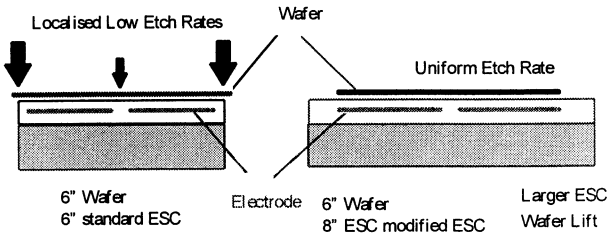


Fig. 6 Modified ESC for uniform RF coupling

TEMPERATURE UNIFORMITY

For silicon processing good temperature uniformity is attained by distributing helium (at pressures between 6 - 15 Torr) between the wafer and the ESC via grooves in the surface, but when used for GaAs the grooves can cause etch rate variations. One option is to remove the grooves altogether, and for non-critical etches this has proven a viable solution. However for more sensitive etches, or those requiring high power for throughput reasons, an ungrooved ESC gives poor uniformity and the risk of resist reticulation at the wafer edge. Table I lists data for a dielectric film etch on a GaAs wafer using an ESC with radial He distribution

grooves of varying sizes (the exact groove dimensions are proprietary).

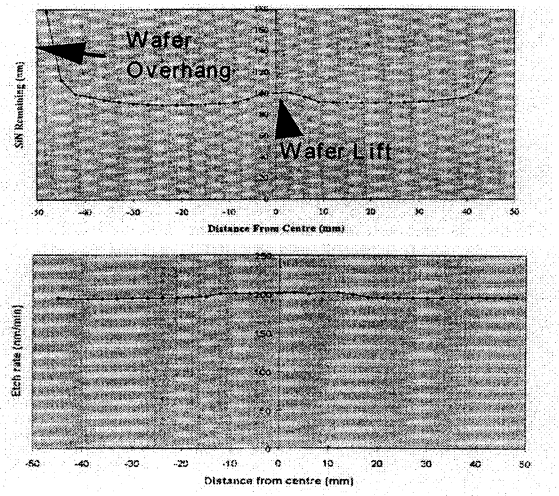


Fig. 7 Effect on etch uniformity of modified ESC for dielectric etch on GaAs

TABLE I
ETCH RATE VARIATION WITH GROOVE SIZE

Size	Variation	Size	Variation
None	0[a]	Medium	-4.2 %
Smallest	-1.2 %	Large	-5.3 %
Small	-3.4 %	Largest (Si)	-9.6 %

[a] resist burns at the wafer edge.

Using a small groove and an oversize ESC gave an etch rate uniformity of 2.1%, with no resist burning, at the required throughput. This illustrates that for GaAs a degree of compromise and flexibility in ESC design is essential to provide a production-worthy solution.

BACKSIDE VIA

Fig. 8 illustrates the case of a GaAs backside via etch where a thinned wafer is bonded to a sapphire carrier. For a thick plate ESC the sapphire carrier thickness is typically of the same order of magnitude as the ESC plate, and has a similar dielectric constant to an alumina ceramic. The Trikon ESC has a wafer blowoff of >30 torr of helium. The clamp force is inversely proportional to the total dielectric

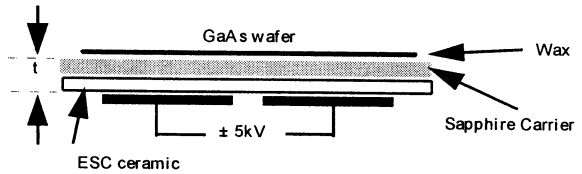
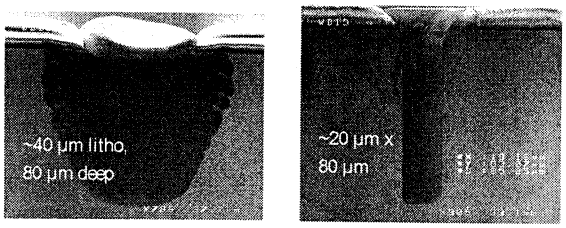


Fig. 8 GaAs backside via on sapphire on thick plate ESC

thickness (t) between the ESC electrode and the GaAs wafer (i.e. force α $1/t^2$). So, adding the sapphire carrier doubles the thickness, t, and results in a blowoff pressure > 7.5 torr. This still constitutes an effective pressure for wafer cooling. This ability to clamp through a sapphire carrier is unique to a thick plate capacitive ESC. For a thin film capacitive ESC the sapphire effectively makes the dielectric an order of magnitude thicker, and the clamp force two orders of magnitude smaller. For a J-R ESC the sapphire does not allow any charge to flow, thus preventing the build up of the voltages required for clamping.. Fig. 9 shows images of isotropic and slot GaAs backside vias. Both processes were done using identical hardware (oversized thick plate ESC in an Omega® 201 ICP chamber).



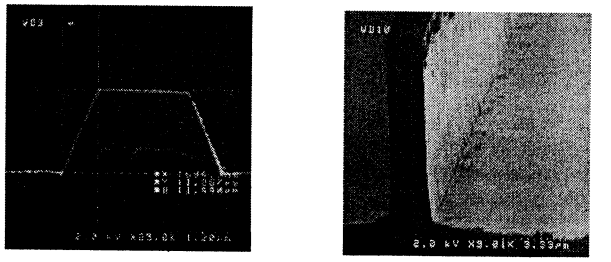
80 mtorr, Cl_2/ CF_4
ER 5.9µm/min ± 5 %
60-70° profile· S_{PR} ~90:1
~2.7 w/h for 125 µm depth

7 mtorr, Cl_2
ER 2.4µm/min ± 5 %
90° profile· S_{PR} ~14:1
~1.4 w/h for 100 µm depth

Fig. 9 Isotropic and slot vias in GaAs etch on identical hardware

HOT ESC

A final illustration of the flexibility of the thick plate capacitive ESC for III-V materials is an application to InP processing. By replacing the metallic parts of the standard ESC with metals that are a thermal expansion match for alumina, it is possible to use the same design up to 250°C. Fig. 10 shows the effects of temperature on InP etching. Not only is it possible to control the profile, it is also possible to attain extremely high etch rates. All the adaptations discussed above can be applied to the hot ESC although at the time of writing requirements to do so have been limited.



Chemistry, Cl_2/Ar, Temp 40°C
ER, v0.85µm/min, Slope ~63°, S_{ox} 4.5:1

Chemistry Cl_2/Ar, Temp 240°C,
ER 7.9µm/min, Slope ~90°, S_{ox} 27:1

Fig. 12 Profile control and enhanced etch rate for InP on a hot ESC.

CONCLUSIONS

The adaptation of ESCs to the processing of GaAs has been demonstrated. It is possible to overcome all the difficulties initially encountered when GaAs processes were run an ESC developed for silicon. As for silicon, it is likely ESCs will eventually replace mechanical clamps for III-V applications.