A Field Plate Device by Self-Aligned Spacer Process

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Abstract

A self-aligned spacer processing method was successfully developed and integrated to Motorola's pHEMT process flow to make a field plate pHEMT device. This process method ensures registration requirement of less than 0.4 μm between field plate and gate is met. The fabricated field plate pHEMT device exhibited improved gate-drain breakdown voltage compared to the non field plate device, 47 V versus 39 V. In addition, preliminary RF data on a 12.6 mm field plate connected to the source device at 3.5 GHz showed 39.8 dBm output power with 11.8 dB associated power gain and 57.2% power added efficiency when biased at 16 V.

INTRODUCTION

There has been great interest in developing GaAs based FETs for base station power amplifier applications. In order to take advantage of available high supply voltage, GaAs FETs must operate at high voltages. The limiting factor for high voltage operation is breakdown voltages of the devices. The field plate (FP) has been proposed and demonstrated to improve breakdown voltages for GaAs FETs [1-2].

A field plate, located between gate and drain electrodes but adjacent to the gate, will extend the depletion edge from the gate-drain edge to the semiconductor region under the field-plate, and shift the peak electric field from the gate edge in the semiconductor to the field plate edge in the dielectric, and reduce the electric field at the gate-drain edge. Consequently, thermionic field emission current and tunneling current from the Schottky gate can be reduced significantly, resulting in a higher gate-drain breakdown voltage. In addition, surface trap effects can be suppressed dramatically, resulting in an increased available RF current at the open channel condition. With the improved off-state gate-drain breakdown voltage and on-state maximum RF channel current, field plate device can potentially operate at higher bias voltage with higher power density.

Physical device simulations indicated that if the gate to field plate spacing is less than 0.4 μm, the advantage of shifting peak electric field will be preserved. On the other hand, if the spacing is more than 0.4 μm, the Schottky gate will encounter premature breakdown because the field plate electrode will not protect the depletion edge at the gate-drain corner in the semiconductor. This breakdown improvement by field plate design is very sensitive to the gate to field plate spacing and less sensitive to the field plate length and the dielectric thickness.

The 0.4 μm registration requirement between the field plate and gate is difficult to implement with current photo process equipment in CS1. In this work, we have developed a self alignment method in conjunction with dielectric spacers to isolate the gate and field plate. The self-aligned field plate processing method ensures that the registration between the field plate and the gate is less than 0.4 μm. This process method is applied to an AlGaAs/InGaAs pHEMT device, and the fabricated FP-pHEMT with FP connected to the source showed improved gate-drain breakdown voltage and power gain.

SELF-ALIGNED FIELD PLATE DEVICE PROCESS

FP device fabrication process is based on the standard AlGaAs/InGaAs pHEMT process [3]. Registration between the gate and field plate is achieved by creating an over sized field plate that extends into where the gate channel will be later created. During the gate channel etch, the portion of the field plate that extends into the channel is trimmed back to the desired size as part of the channel etch. In this manner the field plate structure will always terminate precisely on the drain side of the gate channel.

New process modules were developed to: (A) form an embedded field plate gate metal TiWN; (B) etch a portion of the FP metal during the gate channel etch; and (C) form a dielectric spacer inside gate channel. Fig. 1 (a)-(f) illustrate several important process steps in making the field plate device with the self-aligned spacer process.

A. Embedded Field Plate Metal

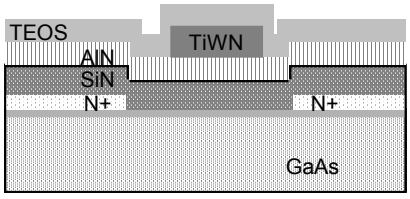
TiWN field plate metal is a blanket reactively sputtered metal film deposited on a dielectric stack of Si_3N_4 and AlN, after the formation of N+ epitaxial region and the isolation implant. Field plate metal stripe was then formed by fluorine based dry etch (Fig. 1(a)). Afterwards, the Au based ohmic contact was formed by using standard lift-off techniques and the subsequent alloy annealing (Fig. 1(b)).

B. Gate Channel Etch

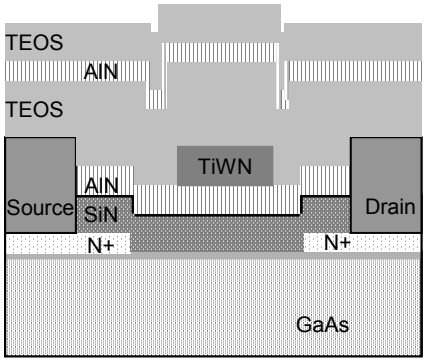
During the gate channel process, TEOS, AlN, TEOS, and field plate TiWN were sequentially etched using photo resist as primary mask. The AlN layer underneath the TiWN FP metal was used as the etch stop layer for both TEOS and TiWN etch (Fig. 1(c)). Subsequently, Si_3N_4 was removed using a C_2F_6 based dry etch that stops on GaAs. During this Si_3N_4 etch step, TEOS layer on the top surface was partially removed (Fig. 1(d)).

C. Si_3N_4 Spacer Formation

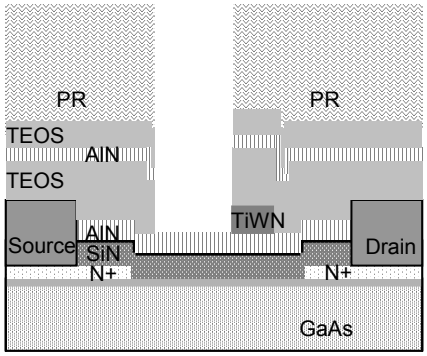
After gate channel formation, a spacer was formed by Si_3N_4 PECVD deposition, and anisotropic C_2F_6 based plasma etch (Fig. 1(e)). TiWN gate metal was deposited to fill the trench and make a Schottky contact to GaAs at the bottom of the trench, followed by metal 1 Au plate (Fig. 1(f)).



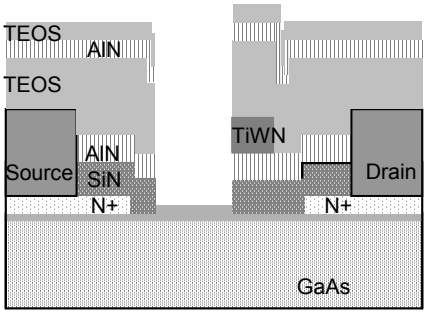
(a) Embedded field plate metal TiWN



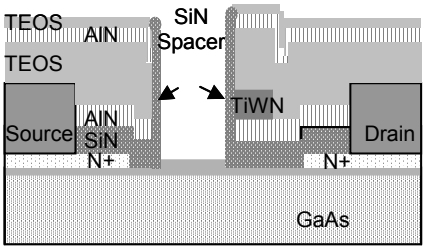
(b) Standard ohmic lift-off process and AlN cap deposition



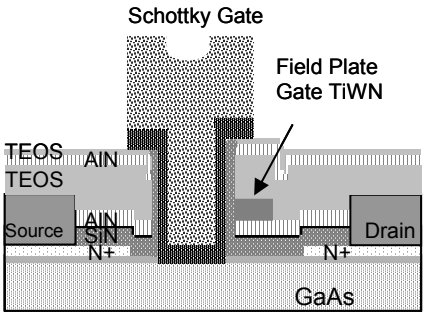
(c) TEOS, AlN, TEOS, and field plate TiWN etch at gate channel clear



(d) Si_3N_4 dielectric etch at gate channel clear



(e) Si_3N_4 inside spacer deposition and etch



(f) Gate metal deposition and metal 1 Au plating

Fig. 1 Several important process steps in making a field plate device using a self-aligned spacer process.

In this self-aligned spacer process, the registration between gate and field plate is controlled by Si_3N_4 film deposition and side wall etch, which can be made much smaller than the required 0.4 μm. In the end, a field plate device was made by a self-aligned spacer process that is integrated into Motorola's standard pHEMT process flow. Fig. 2 shows a cross sectional image of the FP-pHEMT gate formation. This finished device has gate length 0.7 μm, field plate length 0.52 μm, and FP to gate spacing of 0.152 μm.

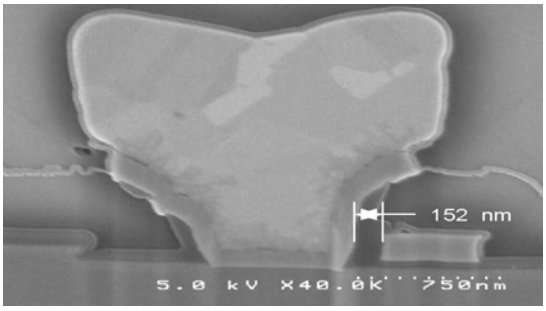


Fig. 2 Cross sectional SEM image of a field plate device made by self-aligned spacer process.

DC AND RF PERFORMANCE

The field plate device is a four terminal device in contrast to a conventional three terminal FET. Field plate terminal can be connected to gate or source, or be an independent electrode. When the FP is connected to the gate through interconnect metal layers, the spacing between gate and FP becomes less critical. When the FP is connected to the source through interconnect metal layers, process imperfection between gate and FP may create an extra leaky path from gate to source, resulting in a low gate-source breakdown voltage or a low Schottky barrier height. Therefore, a FP connected to the source device will be used in the following to demonstrate the process integration.

I-V characteristics of a 2x100 μm device with 1 μm gate length and 0.6 μm field plate length layout dimensions are shown in Figure 3. Typical DC parameters of a FP connected to the source FP-pHEMT are listed in Table I. Data for the standard pHEMT is listed as well for comparison purposes. As can be seen, Idss, Vth, gate-source breakdown (Bvgso), and Schottky barrier height of the FP-pHEMT are similar to the standard pHEMT, indicating that the process integration has been successful and the standard device without FP was not altered by the introduction or modification of process modules described in the previous section. On-resistance increases from 2.5 Ω-mm to 2.86 Ω-mm because of the extended depletion region underneath the FP metal inside semiconductor. Gate-drain breakdown voltage (Bvgdo) is improved from 39 V to 47 V as expected from the FP design.

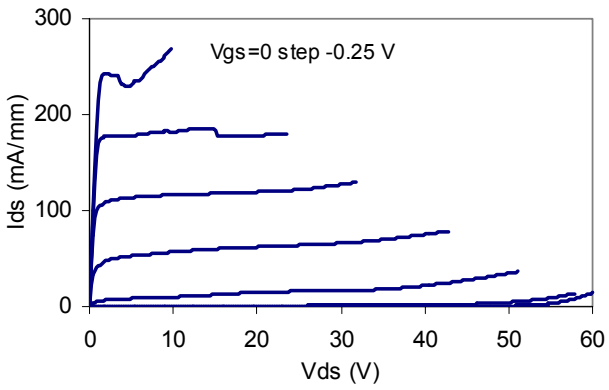


Fig. 3 IV characteristics of a 2x100 μm device with layout gate length 1 μm and field plate length 0.6 μm. Field plate is connected to the source electrode.

Table I. DC Data Comparison

Parameter	pHEMT	FP-pHEMT
Idss (mA/mm)	236	242
Vth @ 1mA/mm (V)	-1.03	-1.04
Bvgso @ 1mA/mm (V)	24	23
Barrier Height (V)	0.8	0.79
On-resistance (Ω-mm)	2.50	2.86
Bvgdo @ 1mA/mm (V)	39	47

Preliminary RF power data on a 12.6 mm FP connected to the source FP-pHEMT device with 0.6 μm field plate length and 1 μm gate length layout dimensions were taken at 3.5 GHz, Vds=16 V, Ids=112 mA. As seen in Fig. 4, at 1dB compression power level, this FP-pHEMT device showed 11.8 dB gain, 39.8 dBm output power with 57.2% associated power added efficiency. In comparison, a non-FP pHEMT device processed on the same wafer had 11.0 dB gain, 40.0 dBm output power with 57.6% PAE. Gain improvement of a FP connected to the source FP-pHEMT device versus a pHEMT device was observed from small signal s-parameter measurement as well.

We also tried to evaluate and compare the maximum bias voltage between FP-pHEMT devices and non FP pHEMT devices because the ultimate goal of developing a FP device is to improve the maximum operation voltage capability. However, a fair comparison is difficult because of the layout dimension differences. Further process and epi structure optimization is on-going to improve the maximum operation voltage capability of FP-pHEMT devices.

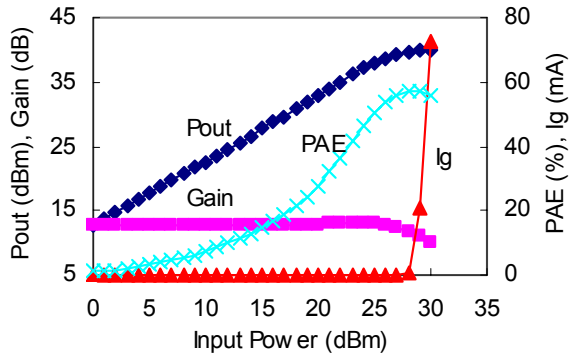


Fig. 4 Output power (Pout), Gain, power-added-efficiency (PAE), gate current (Ig) of a 12.6 mm FP connected to source FP-pHEMT device biased at 16 V and 112 mA operated at 3.5 GHz.

CONCLUSIONS

A field plate pHEMT device was successfully made using a self-aligned spacer processing method integrated into a standard pHEMT process flow. New or modified process modules include embedded field plate metal, gate channel etch, and Si_3N_4 spacer formation. Registration requirement of less than 0.4 μm between the field plate and gate was met by spacer deposition and the subsequent etch back. The fabricated field plate pHEMT device exhibited improved gate-drain breakdown voltage compared to the non field plate device, 47 V versus 39 V. In addition, preliminary RF data on a 12.6 mm field plate connected to the source device at 3.5 GHz showed 39.8 dBm output power with 11.8 dB associated power gain and 57.2% power added efficiency when biased at 16 V. Compared to a non FP-pHEMT device operated at the same condition, power gain improved by 0.8 dB.

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ACRONYMS

FP: Field Plate
pHEMT: pseudomorphic High Electron Mobility Transistor
FETs: Field Effect Transistors
SEM: Scanning Electron Microscope
CS1: Compound Semiconductor One fab in Motorola Inc.
Idss: Drain Saturation Current
Vth: Threshold Voltage
Bvgdo: Gate to Drain Breakdown Voltage
Bvgso: Gate to Source Breakdown Voltage
Pout: Output Power
PAE: Power Added Efficiency