High-Yield Silicon Carbide Vertical Junction Field Effect Transistor Manufacturing for RF and Power Applications

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Abstract

Silicon Carbide ion-implanted vertical junction field effect transistors have been manufactured for high-frequency and high-power applications. The epitaxial parameters, processing and design are being optimized for high yield manufacturing. Self-aligned processing and high resolution lithography enable vertical sidewalls, sub-micron linewidths and uniform metallizations. Optimized oxide passivation techniques allow for low leakage currents and sharp onsets of gate-to-source reverse breakdowns. Dielectric layers provide device isolation and reliability. Floating guard-ring widths, spacings and numbers have been optimized for high-voltage blocking at low resistance. The functional yields for high-frequency VJFETs were in the 78-88% range, for an eight wafer lot. The high-power VJFET functional yields were in the 75-85% range for a four wafer lot. The wafers exhibited excellent performance parameter uniformity. High-power VJFETs are capable of blocking 1.6 kV with a relatively low associated specific-on resistance of 2.1 mΩ cm² (V²br / R on,sp = 1.2 GW/cm²). The VJFETs are scaled to increase current output and have been connected in the cascode configuration to form +1200 V blocking, all-SiC, normally-off power switches.

INTRODUCTION

Silicon Carbide (SiC) is ideally suited for high-power and high-frequency applications due to its high critical field strength, its high saturated drift velocity, its relatively low dielectric constant, and its high thermal conductivity. The wide bandgap of SiC makes device operation possible at temperatures and current-levels well above those of Si devices. The high critical field strength of SiC, which is ten times that of Si, allows high voltage blocking layers to be fabricated significantly thinner than those of comparable Si devices. Thus, SiC devices have lower resistance and are faster as the signal has a shorter distance to travel. Overall, the key advantages of SiC devices over those made of silicon are the lower on-state resistance R on,sp and equivalent voltage blocking, and the potential for higher operating speeds.

In this paper, we report on the high-yield manufacturing of unipolar ion-implanted SiC Vertical Junction Field Effect Transistors (VJFETs) for high-power and high-frequency applications. The processing parameters are being optimized and functional yields in the 77-88% and 75-85% range have been achieved for UHF and power VJFETs, respectively. The high-power VJFETs are capable of blocking up to 1600 V with a relatively low associated specific-on resistance of 2.1 mΩ cm² and a V²br / R on,sp equal to 1.2 GW/cm², [1]. This device performance is close to the limit defined by the physical properties of the SiC material, Fig. 1 [2]. High-power VJFETs have been connected in the cascode configuration to form switches. The all-SiC cascode switches are voltage-driven, and have exhibited excellent power switching characteristics including low-on resistance, high speed, low switching losses, and excellent dynamic operating area in inverter emulation circuits [3].

DEVICE FABRICATION

p+ ion-implanted VJFETs were fabricated in 4H-SiC with a channel layer doped to low 10^15 cm⁻³, and a drift layer doped to mid 10^15 cm⁻³. To achieve +1200 V blocking, the drift layer has a thickness of 12 µm for the high-power VJFETs. Low resistance and capacitance considerations set the high-frequency VJFET drift layer thickness in the 2.5 to 3.5 µm range. The substrates and epitaxy were grown by commercial vendors. A cross section schematic of the VJFET structure is shown in Fig. 2. In the on-state, majority carriers

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(electrons) flow vertically from source to drain. To control the current through the device a voltage is applied to the gates, which adjusts the width of the depletion regions between the p-type gates and the n-type channel.

To mitigate the risk of material defects rendering larger devices inoperative, each 0.0295 cm$^2$ die is divided into five cells. The active cell area is $1.23 \times 10^{-3}$ cm$^2$, excluding the guard ring structure. Dividing a die into cells minimizes the impact of micropipes and other defects on yield. Die can be packaged in parallel, as shown in Fig. 3, to scale current to desired levels.

Precise reactive-ion etching enabled deep and vertical source-pillar sidewalls with minimal roughness, Fig. 4. Techniques were developed to accurately control the pillar etch depth, a crucial parameter for satisfactory device performance.

High resolution lithography enabled sub-micron linewidths with repeatability and high precision, Fig. 5. Electron beam lithography was used to pattern linewidths below 0.4 μm. Resist thicknesses were dictated by linewidth and etch-depth requirements. The ion-implantation signature is visible in Fig. 5 after high temperature implant activation and damage annealing has been performed.

Low resistivity ohmic contacts are essential for high-frequency and high-power operation, where parasitic resistance limits the maximum frequency and causes excessive Joule heating and failure of the devices. In addition, high-temperature and high-power requirements dictate that the contacts must be reliable under extreme conditions. To minimize resistance and assure reliability, metallurgical layer compositions, thicknesses, and lift-off techniques were carefully optimized. The wafer surfaces were cleaned to remove contaminants and acidic wet-etches removed native oxides prior to metallization. A Nickel metal layer, which forms nickel silicide under controlled rapid thermal-anneal treatment, is shown at completion of lift-off in

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**Figure 2.** Cross-section schematic of a Normally-On Ion-Implanted SiC VJFET.

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**Figure 3.** SiC Normally-On Ion-Implanted VJFET test package.

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**Figure 4.** Precise processing enables deep and vertical sidewalls.

High resolution lithography enabled sub-micron linewidths.

**Figure 5.** High resolution lithography enables sub-micron linewidths.

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The use of dielectrics to separate the source from the gate metals virtually eliminates shorting and assists in high quality silicide formation. Techniques to produce photoresist profiles favorable to metal lift-off were successfully employed. As a result, smooth metal profiles were obtained with minimal metal-tear and “wing” formations, Fig. 6.

To overcome the effects of electric field crowding at the device’s edges and exceed 1200 V blocking voltage specification, floating guard-ring structures were used as planar edge termination. In multiple floating guard ring design, the doping level, the proximity of the first guard ring to the main junction, the widths of the rings, and their number and spacings, are critical parameters in maximizing the blocking voltage. The guard ring structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions (rings). The p+ guard rings were formed by multiple ion-implinations, simultaneously with the implantation of the p+ gate. Implant activation and damage thermal-annealing was subsequently performed. Resist guard rings, used for the creation of dielectric isolation regions for ion-implantation are shown in Fig. 8.

A number of dielectric layers with varying thicknesses are superimposed to provide device isolation and enhanced reliability, Fig. 9. Standard lithography and RIE were used to open windows for interconnect metallization.

TESTING AND YIELDS

After implant anneal, the surfaces were passivated by sacrificial oxidation. Combinations of thermal and high-temperature densified CVD oxides were used in various stages of processing. Wet cleanings and short surface RIEs were performed to remove residues. As a result well
passivated surfaces were obtained, as evidenced by the very low leakage currents and the very sharp onsets of reverse breakdown, Fig. 10.

The eight-wafer high-frequency lot had gate-to-source yields in the 77-88% range, Fig. 11. Functional yields for the four-wafer high-power lot were in the 75-85% range.

Process optimizations led to excellent wafer uniformity. This is evident in the gate-to-source forward voltage and drain-to-source resistance histograms of Fig. 12. Forward voltage values below 2.2 V correspond to failed devices.

CONCLUSIONS

High-frequency and high-power 4H-SiC ion-implanted VJFETs were manufactured with high-yields and excellent uniformity. The processing techniques are being optimized for yield, reliability under extreme conditions, fast cycle times, and high volume. The high-power VJFET’s blocking vs. specific-on resistance performance is close to the limit defined by the physical properties of the SiC material. VJFETs have been connected to form all-SiC cascode switches for power conditioning applications.

Figure 10. Low gate-to-source leakage current with sharp onset of reverse breakdown.

Figure 11. Gate-to-source breakdown voltage wafer map showing a yield of 88%.

Figure 12. Gate-to-source forward voltage and drain-to-source resistance histograms, showing good wafer uniformity.

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ACRONYMS

NGC: Northrop Grumman Corporation
Si: Silicon
SiC: Silicon Carbide
VJFET: Vertical Junction Field Effect Transistor
RIE: Reactive Ion Etching
CVD: Chemical Vapor Deposition