Release for production of a 150GHz, 125nm gate 40% In Metamorphic GaAs HEMT MMIC process


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Abstract
This paper deals with the release for production of a 150 GHz, 125 nm gate 40% In metamorphic GaAs HEMT MMIC process. It includes a discussion on the importance of the process development sequence in ensuring a production release. Key points are the objective performance definition and the understanding of the critical process parameters so as to establish an effective control plan vital for a good process control in production.

Introduction
After the market collapse in 2000 the demand for millimetre wave and high speed IC’s is increasing again and with it the need for state of the art performance in industrial manufacturing processes. In this respect OMMIC has developed a new MHEMT process which represents an excellent approach for high gigabit and millimetre wave applications [1] and complements OMMIC’s 100 GHz PHEMT process.

The purpose of this paper is to describe the successful production release of a 150 GHz, 125 nm gate 40% In metamorphic GaAs HEMT MMIC process.

This MHEMT process has recently demonstrated state of the art performance MMICs [2] such as a 3 stage 30GHz LNA designed by the “Centre National d’Etudes Spatiales” exhibiting 28 dB gain with 1.2 dB associated noise figure over a 10GHz bandwidth.

Process development conditions for a successful transfer to production.
When developing a new process for manufacturability it is essential to build on the existing foundry competences and strengths in order that development people only focus on the required new processing steps rather than developing a completely new process. The first thing is therefore to clearly identify these specific steps and the existing ones requiring some modifications before starting a new development. It is also necessary to check that these new steps do not affect the overall reliability. This pragmatic approach undoubtedly permits to achieve at the end the best combination of performance, price and timing without affecting the manufacturing performance.

At the beginning of this work the challenge was to extend the ft performance of OMMIC’s 100 GHz, 135 nm gate 26% In GaAs PHEMT D01PH process up to 150 GHz while maintaining a high degree of manufacturability and a robust process. To achieve this target a metamorphic structure using a composite channel and a single doping plan leading to the same ns (3.25 \(10^2\) cm/s) but with a higher channel In content (40%) was selected (figure 1).

Table 1- Process sequence of a PHEMT/MHEMT process

<table>
<thead>
<tr>
<th>mask layer</th>
<th>OMMIC process description</th>
<th>(development required)</th>
<th>MHEMT/PHEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-LI</td>
<td>Layer Isolation</td>
<td>mesa+boron III</td>
<td>yes</td>
</tr>
<tr>
<td>2-OH</td>
<td>Ohmic contact</td>
<td>yes</td>
<td>(alloying conditions)</td>
</tr>
<tr>
<td>3-GM</td>
<td>Gate Metallisation</td>
<td>yes</td>
<td>(recess etching)</td>
</tr>
<tr>
<td>4-BE</td>
<td>capacitor Bottom Electrode</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>5-CG</td>
<td>Contact to Gate S13N4 via</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>6-TE</td>
<td>capacitor Top Electrode</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>7-CO</td>
<td>Contact Opening S13N4 via</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>8-IN</td>
<td>interconnected metal</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>9-CB</td>
<td>Contact Bonding S13N4 via</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>10-VH</td>
<td>Backside Via Hole</td>
<td>yes</td>
<td>(metamorphic buffer etching)</td>
</tr>
<tr>
<td>11-CS</td>
<td>Chip Separation</td>
<td>no</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1. MHEMT epitaxial structure
acid-H2O2 mixture in order to take advantage of the high selectivity between the GaInAs cap and the AlInAs Shottky barrier layer.

Optimal pinch-off voltage
The Schottky barrier layer thickness was experimentally defined to achieve a typical extrinsic ft of 150 GHz (figure 2a and 2b).

Optimal pinch-off voltage
#Figure 2a.  Extrinsic ft versus Vt

Finally it was considered that a 120 Å thick Schottky layer represented a good trade-off to achieve 150 GHz ft. A typical I-V curve of the MHEMT device is shown in figure 3. Optimization of the composite channel has resulted in near kink free behaviour with good drain to source breakdown voltage (>9V).

Via hole etching
For the conventional GaAs PHEMT process, via hole etching is achieved by a combination of Cl₂ based RIE plasma and wet etching. Because the metamorphic buffer acts as an etch stop for dry etching, an additional HCl based mixture was added.

Establishing a control plan
Compared with the production PHEMT only a limited number of processing steps are changed. The gate etching is highly selective and therefore very well controlled. Hence the emphasis is placed on the control of the gate length as well as a good control of the starting epi layer resulting in a robust control plan.

The other parameters to be kept under control are the same as for the production PHEMT process and include the resist, dielectric, metal thicknesses, etc...

The mains parameters such as the threshold voltage( Vt) are in control from batch to batch thanks to selective etching. The threshold voltage on more than 20 wafers from 4 different epitaxial runs is shown in figure 4.

On a RF reliability demonstrator circuit (DEC: dynamic evaluation circuit), shown in figures 5 and 6, NF min and associated Gain were measured on 36 samples, as a result of the threshold uniformity on wafer, the histogram of NF min and associated gain at 12 GHz from 36 DECs is quite satisfactory (Fig.7 and 8).
The noise figure of the DEC is mainly related to the biasing resistors and is not representative of the intrinsic noise performance of the process. In particular, the NF min of the process at 30GHz has been measured to be 0.8dB which is fully in line with the LNA results mentioned in the introduction (figure 11).

Process reliability qualification

Examples of 1000h 225°C storage test and 175°C endurance tests are respectively shown in figures 9 and 10.

Some more endurance tests are made on DECs (figures 5 and 6) from CNES wafers and give good results on NF min and associated Gain at 12 GHz (figures 11 and 12).
Conclusion: This paper reports on a cost effective and efficient approach for a successful transfer into production of a 125 nm gate length 40 % MHEMT process. The authors demonstrate the importance of capitalizing on an existing PHEMT process currently in production in order to effectively limit the number of new processing steps to be transferred.

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Indexing terms: MHEMT transistors, millimetre wave devices, MMIC’s

References:
[3] 0.15µm In0.4 GaAs/InAlAs Metamorphic HEMT’ s (M-HEMT’s) using a novel triple shaped gate structure assisted by PMGI resist. Dae-Hyun Kim, Suk-Jin Lee, Ki-Woong Chung, and Kwang-Seok Seo. Digest of papers 2004 International conference on Gallium-Arsenide MANufacturing TECHnology.