AlGaN/GaN High Electron Mobility Transistors and Diodes Fabricated on Large Area Silicon on poly-SiC (SopSiC) Substrates for Lower Cost and Higher Yield

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ABSTRACT

The dc and rf performance of AlGaN/GaN High Electron Mobility Transistors (HEMTs) grown by Molecular Beam Epitaxy on Si-on-poly-SiC (SopSiC) substrates is reported. The HEMT structure incorporated a 7 period GaN/AlN superlattice between the AlGaN barrier and GaN channel for improved carrier confinement. The knee voltage of devices with 2 µm gate-drain spacing was 2.12 V and increased to 3 V at 8 µm spacing. The maximum frequency of oscillation, f_{MAX}, was ~40 GHz for devices with 0.5 µm gate length and 2 µm gate-drain spacing. Parameter extraction from the measured rf characteristics showed a maximum intrinsic transconductance of 143 $mS.mm^{-1}$.

INTRODUCTION

GaN and related alloys are typically grown on either sapphire or SiC substrates. The GaN has a significant lattice mismatch with both types of substrates, leading to a high density of threading dislocations in the nitride layer. The use of SiC substrates is preferred for electronic devices such as High Electron Mobility Transistors (HEMTs) because of the superior thermal conductivity, leading to less device self-heating and improved reliability and operating stability. AlGaN/GaN HEMTs grown on SiC substrates are very promising for high power, high temperature applications in telecommunications, hybrid electric vehicles, power flow control and remote sensing.

GaN-based electronics is in the initial stages of commercialization for power amplifiers dedicated to next generation wireless infrastructures, including World Interoperability for Microwave Access (WiMAX) base stations, and also for hybrid electric vehicles, power flow control and defense applications [1-10]. GaN-on-silicon field-effect transistor technology enables base station equipment manufacturers to optimize bandwidth, power and efficiency at attractive sizes and costs [9,11-15]. In particular, the WiMAX market requires demanding combinations of power, efficiency, frequency (typically 2.3-2.9 GHz and 3.3-3.8 GHz) and bandwidth that are beyond the specifications of existing GaAs and Si devices. The use of 100mm silicon wafers allows scaling to produce statistically significant reliability data, to use proven packages from the silicon industry and to quickly scale-up volume production. However, SiC substrates would be preferred because of their superior thermal conductivity but the cost of large area single-crystal SiC is prohibitive. The use of silicon-on-polycrystalline SiC provides an alternative by combining the low cost approach of the silicon and poly-SiC bulk with better thermal dissipation [10,16,17]. An intriguing approach involves the use of the Smart Cut™ technology already demonstrated in large volume industry (SOI substrates) to produce SopSiC substrates [10,17]. The AlGaN/GaN HEMT wafer is then grown on the silicon on poly-SiC (SopSiC) composite substrate. The thermal conductivity of the composite SopSiC substrate is comparable to that of polycrystalline SiC and superior to Si. For power amplifier applications, ability to extract heat and the allowed thermal budget of operation is critical. High thermal conductivity substrates may make it possible to design a power amplifier without an auxiliary cooling system and lead to further cost savings (materials/operation) along with weight/volume reduction.

Initial results have shown excellent dc breakdown and rf performance of AlGaN/GaN HEMTs on SopSiC substrates. In this paper we report on improved structures using GaN/AlN superlattice confinement layers above the GaN channel. The devices exhibit low parasitics, which are needed for good rf performance and low knee voltages.

EXPERIMENTAL

The starting substrates were 4 in. diameter high resistivity (111) Si and conducting polycrystalline SiC. The Si was initially oxidized and implanted with a high dose of H^+ ions, cleaned, and bonded to the SiC wafer. Removal of the Si by Smart Cut™ splitting was followed by reclaiming of the top Si wafer and surface preparation of the SopSiC wafer. The SopSiC wafer consists of the SiC substrate, followed by 0.1 µm of thermal SiO_2, and 0.2 µm of (111) Si. The Molecular

Beam Epitaxy (MBE) growth in the rf N_2 plasma-assisted mode of the HEMT structure began with deposition of an ~0.5 µm thick GaN buffer, 1.4 µm additional buffer of $Al_{0.25}Ga_{0.75}$ N, and was followed by the active regions of a 100 Å thick GaN channel, then a GaN/AlN 10 period superlattice with total thickness 32 nm and average Al content of 32 at.%, a $Al_{0.25}Ga_{0.75}N$ barrier (50 Å) and undoped 20 Å GaN cap layer. The sheet resistance of the HEMT was 456 Ω/ sq, with a sheet carrier density of 7×10^{12} cm^{-2} and electron mobility at 300 K of 1400 cm^2 /V s. A cross-sectional TEM micrograph of the entire structure is shown in Figure 1. The structure shows single crystal nature and clean, sharp interfaces, while there is the usual density (~5 $\times 10^9$ cm^{-2}) of threading dislocations originating from the lattice mismatch at the hetero-interface. A more detailed TEM cross-section is shown at the left of Figure 2. The ~500 µm thick polycrystalline SiC provides electrical isolation, heat dissipation and mechanical strength. This is followed by ~200 nm of SiO_2 which establishes the quality of the wafer bonding and finally ~470 nm of high resistivity (111) Si which provides a suitable surface for growth of hexagonal GaN and also provides electrical isolation. The TEM micrograph at the right of Figure 2 shows a close-up of the GaN/AlN superlattice barrier enhancement region, with excellent layer planarity.

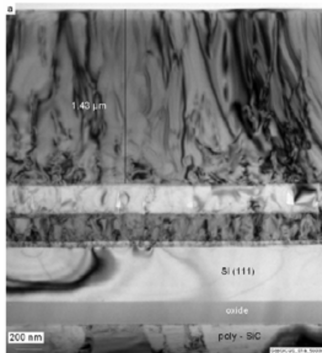


Figure 1.Cross-sectional TEM micrographs of full HEMT-on- SopSiC substrate.

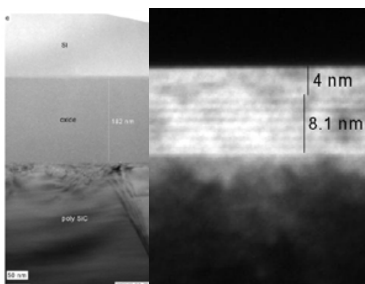


Figure 2. Cross-sectional TEM micrographs of SopSiC substrate(left) and close-up of AlN/GaN superlattice region (right).

Device fabrication began with mesa isolation by Cl_2 /Ar inductively coupled plasma etching (150 W source power, 40 W rf chuck power). Isolation currents were in the low µA at 40 V bias for a mesa depth of 1500Å. Ohmic contacts were formed by lift-off of e-beam deposited Ti/Al/Pt/Au subsequently annealed at 950 °C for 30 s under a flowing N_2 ambient. The specific contact resistance derived from transmission line method measurements was 9×10^{-6} Ω cm^2. Schottky gates with gate length of 0.5 µm and gate widths in the range 200-800 µm multiple finger configuration with electron beam deposited Pt/Au were also patterned by liftoff. The gate width of the unit FET was 100 µm. The gate length was measured by SEM to be 0.52 µm. The HEMT dc characteristics were measured in both dc and pulsed modes using an HP 4145B parameter analyzer for the dc and a pulse generator, dc power supply, and oscilloscope for the pulsed measurements. The rf performance of the HEMTs was characterized with an HP 8723C network analyzer.

DISCUSSION

Figure 3 shows a typical I_{DS}-V_{DS} characteristics from a HEMT. At top, the device 2x100 μm^2 gates with 2 µm gate-drain spacing. All of the devices showed excellent gate-drain breakdown voltages in the range 40-350V for gate-drain spacing of 2-125 µm, where the reverse breakdown voltage was defined as the voltage at which the reverse current density was 1µA-cm^{-2}. These correspond to breakdown fields in the range 3.2-20 $\times 10^4$ V/cm and are comparable to HEMTs on other substrates with the same sheet carrier density. The maximum drain-source current of 400 mA was obtained in an 800 µm gate width HEMT, while the highest current density of 375 mA/mm was obtained in the 200 µm gate width devices.

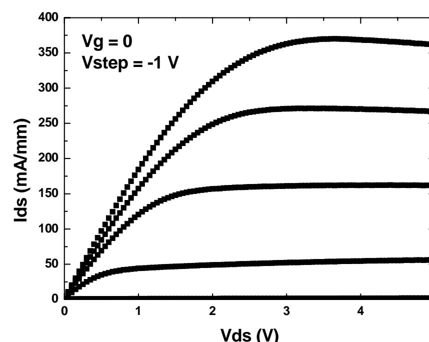
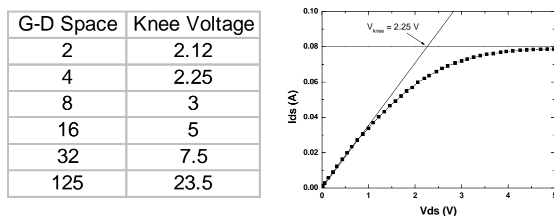


Figure 3.I_{DS}-V_{DS} characteristics from a 0.5 × 200 μm^2 gate length HEMT-on- SopSiC.

We were able to extract the variation in knee voltage as a function of gate-drain spacing from the I_{DS}-V_{DS} characteristics, as shown in Figure 4. A minimum value of 2.12 V was obtained for a 2 µm spacing device. This further confirmed the good electron mobility in the two-dimensional electron channel of the HEMT. With the increase of gate drain spacing, the drain resistance and knee voltage proportionally increased. Figure 5 shows typical transfer characteristics from a 200 µm gate width device with 2 µm gate-drain spacing. The maximum extrinsic transconductance was ~110 $mS.mm^{-1}$. The maximum intrinsic transconductance was of 143 $mS.mm^{-1}$, which was estimated with $\frac{1}{g_{mex}} = \frac{1}{g_{\min}} + \frac{1}{Rs}$, where g_{mex} is the extrinsic transconductance, g_{min} is the intrinsic transconductance and the Rs is the gate-source resistance. The gate source resistance was extracted from the s parameters with an equivalent circuit. The drain current of ~350 $mA.mm^{-1}$ is in line with that expected for this sheet carrier density.



G-D Space	Knee Voltage
2	2.12
4	2.25
8	3
16	5
32	7.5
125	23.5

Figure 4.Extraction of knee voltage from I_{DS}-V_{DS} characteristic for device with 2 µm gate-drain spacing.

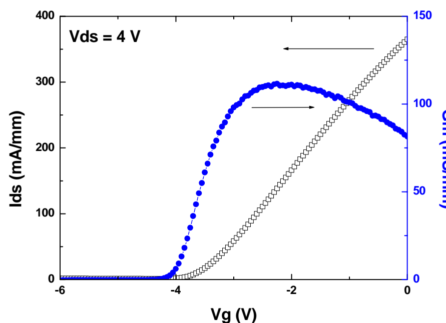


Figure 5. Transfer characteristics from a 0.5 × 200 µm gate length HEMT-on- SopSiC.

One frequently reported problem for AlGaN/GaN HEMTs is that the rf power obtained is still much lower than expected from the dc characteristics[18-23]. This problem is manifested by a collapse in drain current or frequency dispersions in transconductance and output resistance, leading to severely reduced output power and power-added efficiency. Several mechanisms have been identified, including the presence of surface states between the gate and drain which deplete the channel in this region with time constant long enough to disrupt modulation of the channel charge during large signal operation or of trap states in the buffer layer [18-20,23]. Several studies have shown that the use of dielectric passivation layers can be effective in reducing the effects of surface states. We have employed gate lag measurements on surface passivated HEMTs as a metric for establishing the presence of buffer traps[22]. In this method, the drain current (I_{DS}) response to a pulsed gate-source voltage (V_G) is measured. Figure 6 shows the normalized I_{DS} as a function of drain-source voltage (V_{DS}) for both dc and pulsed measurements of a SiN_X passivated HEMT. In the data, V_G was pulsed from –10V to 0 at 0.1MHz and 10% duty cycle. The differences between dc and pulsed drain currents are consistent with the presence of buffer traps. This suggests that further optimization of the buffer growth conditions are necessary.

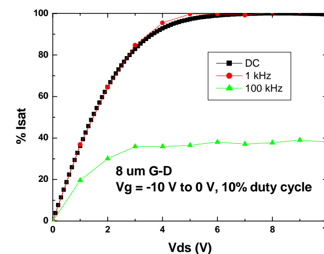


Figure 6.Gate lag measurements from a 0.5 × 200µm gate length HEMT-on- SopSiC with gate voltage pulsed from 0 to –3 V.

The HEMTs-on-SopSiC showed reasonable high frequency performance. Figure 7 shows the rf performance of a 0.5 × 200 $µm^2$ gate length device with 2 µm gate-drain distance . The cutoff frequency (f_T) and maximum frequency of oscillation (f_{MAX}) were extracted from measured s-parameters and measured as a function of gate-to-drain distance and also V_{DS}. The latter data is shown at the right of Figure 7. The f_T values varied from 14-27 GHz for gate-to-drain distances of 2-32 µm with f_{MAX} in the range 40-47 GHz for these conditions. For optimized growth of HEMTs on sapphire Si or SiC substrates with fairly similar sheet carrier densities to those used here, the typical f_T is around 25-30 GHz for 0.3 µm devices using a similar mask layout, with a typical f_{MAX} in the range 50-88 GHz[24,25]. The rf performance of AlGaN/GaN HEMTs is a strong function of gate length (L_G), with a linear f_T vs. L_G^{-1} relationship observed. Karmalkar, Shur and Gaska [26] have noted that transistors with $f_{MAX} > f_T$ can have useful power gains for $f > f_T$ and up to f_{MAX} since a current gain of <1 may be compensated by a voltage gain >1 for $f_T < f < f_{MAX}$. A typical working frequency for MMICs based on HEMTs is expected to be 2/3 f_{MAX}. The fact that f_{MAX} is slightly lower than expected from conventional HEMTs is likely due to additional resistances

or capacitances associated with the SopSiC template and this may be a drawback relative to the standard Si or SiC substrates.

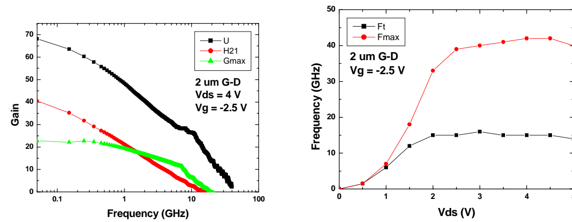


Figure 7. rf performance of a 0.5 × 200 μm^2 gate length HEMT-on- SopSiC (top) and variation of f_T and f_{MAX} as a function of drain-source voltage for a fixed gate voltage of 2.5 V.

CONCLUSIONS

AlGaN/GaN HEMTs fabricated on SopSiC substrates show very promising dc and rf performance and show the potential of this approach to realize low cost, large-area, thermally conducting substrates that are needed to enhance the performance/cost ratio of GaN-based power amplifiers. Further work is necessary to improve the buffer and material quality so that the performance is competitive with AlGaN/GaN HEMTs on sapphire and single-crystal SiC.

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ACRONYMS

HEMT: High Electron Mobility Transistor
SopSiC: Silicon-on-poly-SiC
MBE: molecular beam epitaxy
MMIC: monolithic microwave integrated circuit
SEM: scanning electron microscope
TEM: transmission electron microscope