

MMIC Packaging and Heterogeneous Integration Using Wafer-Scale Assembly

P. Chang-Chien, X. Zeng, K. Tornquist, M. Nishimoto, M. Battung, Y. Chung, J. Yang, D. Farkas, M. Yajima, C. Cheung, K. Luo, D. Eaves, J. Lee, J. Uyeda, and M. Barsky

Northrop Grumman Space Technology
One Space Park, Redondo Beach, CA 90278
Patty Chang-Chien, Email: patty.chang-chien@ngc.com Tel: (310) 812-7432

Keywords: ... Wafer Scale Assembly, Wafer-Level Packaging, Wafer Bonding, Heterogeneous Integration

Abstract

Northrop Grumman Space Technology (NGST) has developed a MMIC compatible, hermetic Wafer Scale Assembly (WSA) technology that is proven to be mechanically and electrically robust. This WSA technology is an enabling technology for realizing lightweight, multifunctional and low cost modules for current and future space and military systems. In this paper, data obtained from various DC/RF interconnect structures as well as packaged MMICs using NGST's 2-layer WSA technology is presented. Furthermore, RF front-end modules with integrated antenna are also demonstrated. Data from the integrated RF module as well as multiple-layer DC/RF structures fabricated in a 4-layer WSA configuration is also presented. NGST's WSA technology enables true three-dimensional circuit integration by allowing intimate multi-function integration among various MMIC technologies and offers significant size and weight advantages to future high performance RF systems.

INTRODUCTION

As future space and military systems continue to demand higher operating frequencies, better system performance, more functionality and system agility, lower module/unit cost and faster system realization, 3D heterogeneous integration at the MMIC wafer level becomes an attractive and enabling technology. NGST's WSA technology offers a unique capability to place multiple semiconductor technologies in close proximity with one another without sacrificing either performance, or reliability or manufacturability from the respective technologies. In this paper, a short description of the wafer scale assembly process is presented, followed by measured results obtained from various DC/RF interconnect structures as well as packaged MMICs using NGST's 2-layer and multiple layer WSA technology.

WAFER-SCALE ASSEMBLY PROCESS

WSA is achieved by stacking multiple layers/wafers vertically by a wafer bonding process. Northrop Grumman Space Technology developed a low temperature wafer bonding process [1-2] that is a batch fabrication process and it is fully compatible with MMIC fabrication. The WSA

process is performed after the standard MMIC processes,, therefore, it preserves the existing high-reliability production process controls already at the Northrop Grumman MMIC production facility. The low temperature wafer bonding process is described in [1-2] and will not be repeated here. NGST has successfully applied this wafer scale assembly process to a number of RF MMIC technologies, including RF MEMS switches [3] and several MMICs in various frequency bands. Some of these MMIC results are presented in later section of this paper.

DC/RF CONNECTIONS WITHIN 2-LAYER WSAs

One important building block for WSA structures is the Intra-Cavity InterConnections (ICICs). They are three-dimensional interconnections within the bonded wafer stack. They are simply vertical posts that connect between the two inner wafer surfaces. The ICICs can greatly reduce losses associated with signal routing between different circuits or functional blocks by eliminating unnecessary wire-bonding between chips hence decreasing the overall routing distances. Low loss, compact ICICs can significantly enhance circuit performance by reducing parasitics in signal routing, enhancing circuit speed, and enabling new circuit architectures.

DC Interconnects

Different DC interconnection test structures were designed to evaluate interconnect performance [4]. These test structures include daisy chains of different lengths and different ICIC diameters and shapes. Based on small daisy chain measurement data [4, 5], DC yield of these ICIC daisy chain structures is consistently greater than 99% with ICIC diameters greater than 30um.

RF Interconnects

RF test structures consist of back-to-back connections were also designed to evaluate the RF characteristics of these ICICs. Figure 1a is an illustration of a back-to-back RF transition test structure designed to operate at X band. The structure consists of two RF via transitions and a through line inside the cavity. Insertion loss of less than 0.2dB is obtained from the entire structure across the band, which indicates that an individual RF ICIC transition has less than 0.1dB loss at X-band.

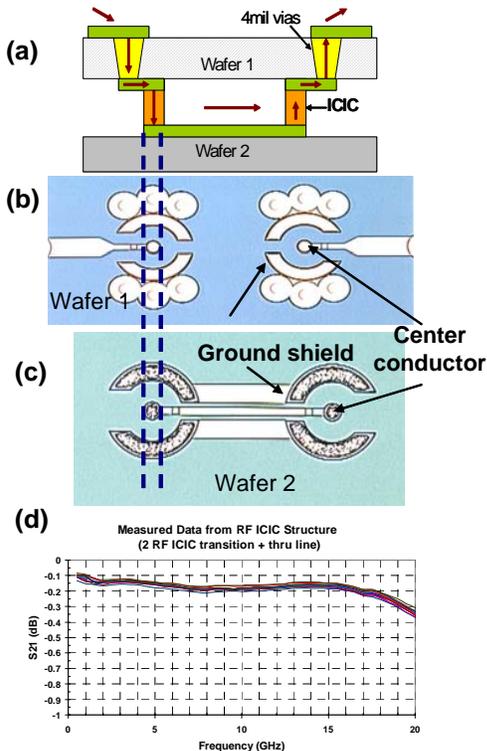


Figure 1. (a) Illustration of the X-band RF transition test structure (b) Photograph of the RF ICIC structure taken from the inner surface of wafer 1 (b) Photograph of the RF ICIC structure taken from the inner surface of wafer 2. (c) Measured data obtained from the ICIC test structure.

Northrop Grumman Space Technology also demonstrated a W-band RF transition with insertion loss less than 0.2dB and return loss greater than 24dB at W-band [6] using these ICICs. The data obtained from the W-band transition is shown in Figure 2. In addition, the ICICs can be utilized to create isolation fences between sensitive circuits and make channelization at the MMIC level possible. To demonstrate this, measurements of a pair of coupled microstrip lines were measured with and without an isolation fence located between them (Figure 3). An average of 30dB of isolation improvement was obtained from this particular isolation fence structure at W-band. Higher levels of isolation can be achieved by adding multiple layers of isolation fences. These configurations were designed but not tested due to limitations in dynamic range of the test setup.

In summary, NGST has demonstrated a high yield wafer assembly process to construct both DC and RF ICIC structures. The ability to construct high yield, low loss interconnects combined with the added circuit design flexibility with these ICICs provides a powerful combination in achieving high performance RF circuits at high frequencies. This ICIC advantage combined with the compact form factor, light weight, heterogeneous integration

and hermetic sealing offered by the wafer-level packaging process can have an unprecedented impact in RF system architecture and future RF modules.

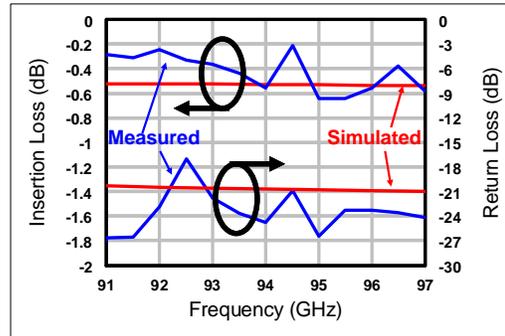
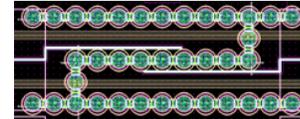


Figure 2. Measured data vs. simulated data obtained from a W-band RF transition.

Isolation Test Structures (w/o fence)



Isolation Test Structures (w/ fence)



Isolation Measurement

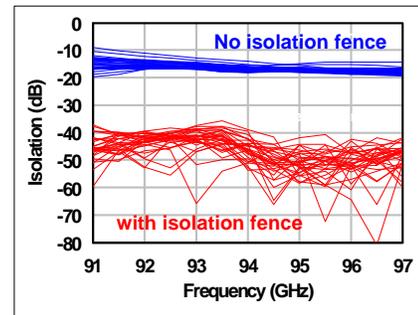


Figure 3. W-band isolation test structures with measured data.

WAFER SCALE MMIC PACKAGING

To demonstrate the MMIC compatibility of NGST's WSA technology, MMICs operate from UHF band up to W-band have been fabricated, packaged, and evaluated. Measured data from some of these packaged circuits are shown in Figure 4. The data confirms that the WSA processes are 100% compatible with existing III-V semiconductor production processes.

MULTI-FUNCTIONALITY INTEGRATION

NGST's WSA technology is an enabling technology for compact heterogeneous integration, both in functionality

integration within a technology as well as integration among different technologies.

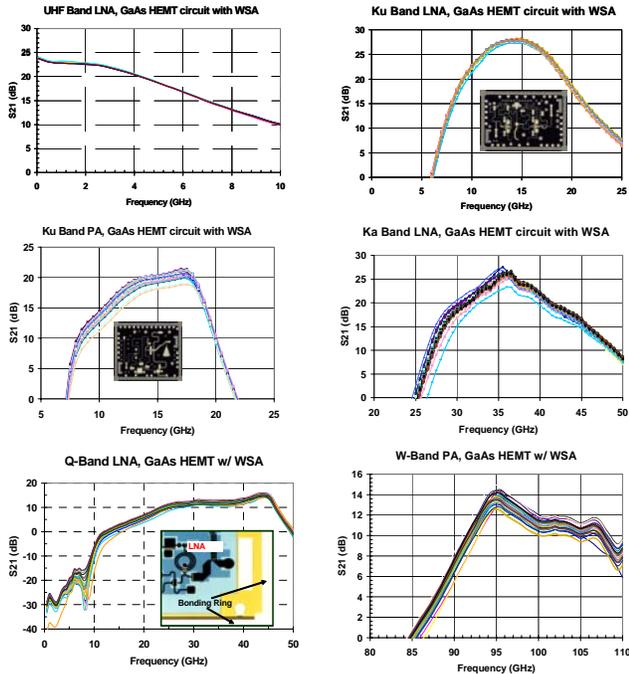


Figure 4. Data obtained from various MMICs packaged using NGST’s WSA processes.

The integrated antenna front end module is constructed by two wafers, which are fabricated individually using standard MMIC fabrication processes. Matching metallic sealing rings around each unit cell are deposited on the two wafers. A low temperature wafer scale bonding process fuses the sealing rings of the two wafers together to form a hermetic cavity, encapsulating the RF circuitries (Figure 5). In this case, the cavity contains a Q-band amplifier, a 3-bit phase shifter and some intra-cavity interconnections (ICICs) to provide RF and DC routings. Photograph of a single cell showing its circuits and the photograph of completed RF front end modules are shown in Figure 6(a) and 6(b), respectively.

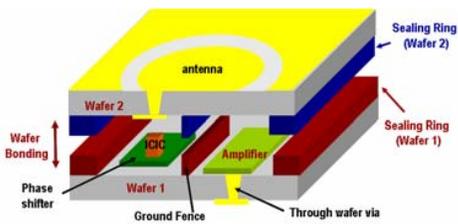


Figure 5. Schematic representation of the antenna RF front end module.

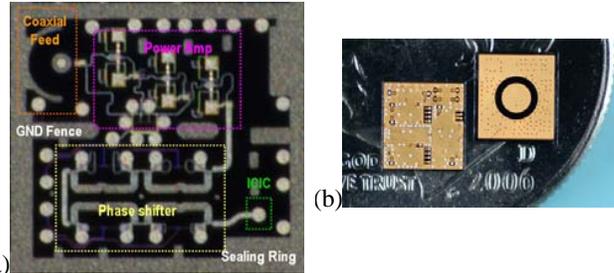


Figure 6. (a) Photograph of a single cell, showing the power amplifier, the phase shifter, the coaxial antenna feed, and the intra-cavity interconnections (ICICs). (b) Photograph of fabricated Q-band RF front end module.

The performance of the RF electronics was verified through on-wafer probe measurement by accessing the probe pads on the backside of wafer 1. The Q-band amplifier is unconditionally stable with 14dB of gain and has input/output return loss of > 15dB. Measured data obtained from the amplifier and the 3-bit phase shifter is shown in Figure 7. The measurement shows good agreement between the measured and predicted performance, showing low RMS phase error.

The functionality of the entire integrated module was confirmed by a bore-sight power measurement from the built-in slot antenna (Figure 8). NGST is currently building a 4-element linearly electronically steerable array (ESA) with these integrated Q band modules to demonstrate the module performance in the relevant system environment.

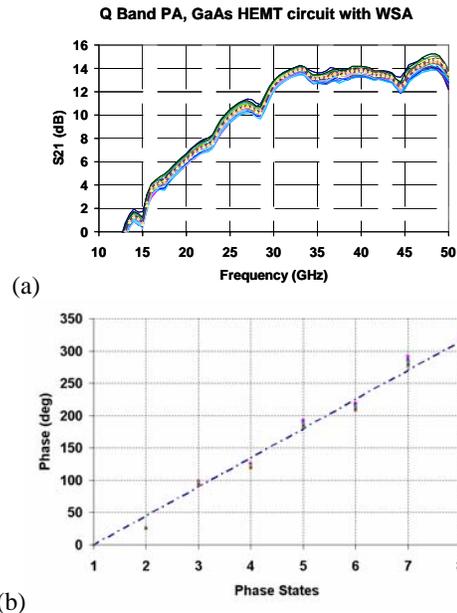


Figure 7. (a) Measured data from the integrated Q-band PA (b) Measured data from the integrated Q-band 3-bit phase shifter.

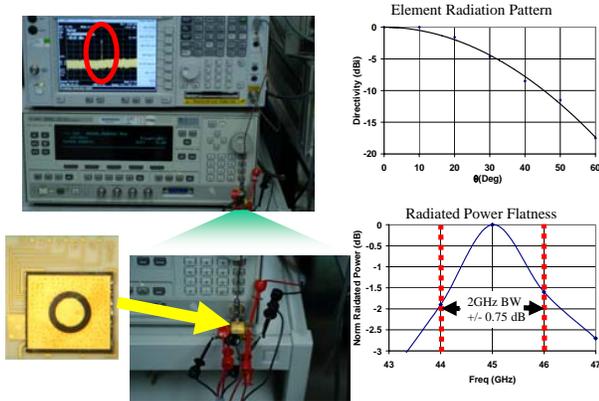


Figure 8. Power measurement obtained from the integrated antenna module assembled using WSA.

MULTI-LAYER MMIC INTEGRATION

NGST also demonstrated multiple-layer WSA by stacking multiple two-layer WSA vertically using the same wafer bonding technology. Details of the assembly processes will not be described here [8]. Continuity test structures, consist of four levels of through-wafer vias and three layers of ICICs in series, were constructed in a four-level wafer stack. These four-layer test structures, spanning across 4 wafers vertically, have functional yields of greater than 90%, which translates to greater than 99% of individual element yield.

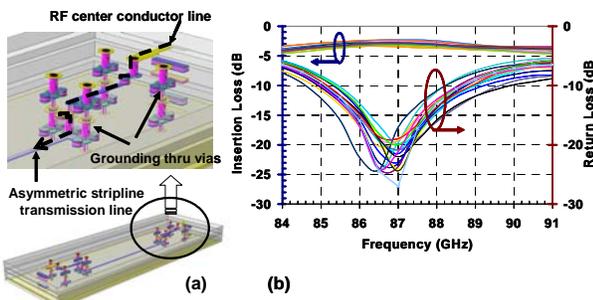


Figure 9. (a) 4-layer RF transition test structures in WSA. (b) data obtained from the 4-layer RF transition test structure

To evaluate RF characteristics of transitions in the four-layer WSA stack, a RF transition structure was designed utilizing an asymmetric stripline transmission line (Figure 9a). Return loss of this four-wafer structure is measured to be >20 dB at 87GHz with narrow bandwidth of 1.5GHz. Insertion loss of this structure is as low as 2.3dB at that frequency (Figure 9b). The insertion loss of vertical transition alone is estimated to be below 1.0dB, the other loss is contributed by the long transmission line (>2.2 mm of metal loss) and poor matching between the WSA layers. Further design optimization is needed to improve the transition characteristics. Both insertion loss and return loss data are tightly grouped from all sites tested across the

wafer. This successful demonstration of the w-band RF transition suggests that the multi-wafer WSA is a feasible method to integrate advanced RF structures into multi-wafer assembly for high frequency RF communication applications.

CONCLUSIONS

MMIC packaging and heterogeneous integration were demonstrated via NGST's WSA technology. It is an enabling technology for compact, high performance, low cost, hermetically sealed RF front end electronics.

ACKNOWLEDGEMENTS

The multi-layer assembly work and the W-band circuit efforts were supported by the DARPA Scalable Millimeter-wave Architectures for Reconfigurable Transceivers (SMART) program and the Air Force Research Laboratory under the AFRL Contract No. FA8650-06-C-7600. The authors wish to thank Mark Calcaterra (AFRL), Paul Watson (AFRL), and Mark Rosker (DARPA) for their support. The authors also wish to thank the entire engineering, processing and testing team at NGST's Microelectronics Product Center for MMIC fabrication, package fabrication and testing.

REFERENCES

- [1] P. Chang-Chien, et al. "Low temperature, hermetic, high-yield wafer-level packaging technology", *Northrop Grumman Technology Review Journal*, spring/summer 2006, vol. 14, number 1, pp. 77-97.
- [2] P. Chang-Chien, et al. "MMIC Compatible Wafer-Level Packaging Technology", *19th International conference on Indium Phosphide and Related Materials (IPRM, 07)*, May 2007, Matsue, Japan invited paper.
- [3] P. Chang-Chien, "MMIC Compatible Lateral Deflection RF MEMS Switches", invited paper, *Symposium "State-of-the-Art Program on Compound Semiconductors XLII" of the 207th meeting of the electrochemical Society*, May 2005, Quebec City, Canada, pp. 301-313.
- [4] P. Chang-Chien, et al. "Dense Intra-Cavity Interconnection Technology for Hermetically packaged MMICs" *Symposium "State-of-the-Art Program on Compound Semiconductors 45"*, *SOTAPOCS 45* Oct. 2006, Cancun, Mexico, paper number 1532.
- [5] M. Yajima, et al. "High Yield Intra-Cavity Interconnection Fabrication Method and Characterization Methodologies" 2007 International Conference on Compound Semiconductor Manufacturing Technology (CSMANTECH), May 2007, Austin TX, paper 8.3.
- [6] D. Farkas, et al. "Demonstration of a Low Loss W-Band Interconnect and Circuit Isolation Structure for Wafer Scale Assembly" *IEEE MTT-S International Microwave Symposium, IMS 2007, Honolulu, Hawaii*, June 2007.
- [7] J. Yang et al. "Wafer level integrated antenna front end module for low cost phased array implementation" *IEEE MTT-S International Microwave Symposium, IMS 2007, Honolulu, Hawaii*, June 2007.
- [8] X. Zeng, et al. "High Performance Wafer-Scale Assembly for III-V Semiconductor MMICs", invited paper, *Symposium "State-of-the-Art Program on Compound Semiconductors XLII" of the 211th meeting of the electrochemical society*, May 2007, Chicago, IL. Paper E5-03500

ACRONYMS

- MMIC: Monolithic Microwave Integrated Circuits
- WSA: Wafer-Scale Assembly
- NGST: Northrop Grumman Space Technology
- ICIC: Intra-Cavity InterConnections
- ESA: Electronically Steerable Array