Development of a Lead Free Solder Bumped RFIC Switch Process

Suzanne Combe, John S Atherton, Matthew F O'Keefe, Chris Main
Filtronic IP, Newton Aycliffe, County Durham, DL5 6JW. UK.
Phone + 44 1325 301111, Fax + 44 1325 306600
email suzanne.combe@filcs.com

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ABSTRACT

As the RF front-end module market aggressively strives to reduce both size and cost of their assemblies, the consumer demands ever-increasing levels of functionality. To accommodate this front-end module makers are looking to more advanced packaging solutions which accommodate the increased pin counts of advancing architectures while also enabling simplified assembly processing.

At Filtronic Compound Semiconductors' 150mm gallium arsenide wafer fab in Newton Aycliffe, a high yielding RF switch process with flip chip capability is being developed for high volume applications. Whilst maintaining the ethos within Filtronic to provide products mindful of regulatory and industry requirements, such as the Restriction of Hazardous Substances Directive (RoHS), and offer Lead (Pb)-Free and environmental considerate solutions to meet the needs of its customers.

This paper will discuss the wafer level process development of a lead free solder bumped process and necessary process controls and wafer level qualification results.

INTRODUCTION

Flip chip bonding is defined as the connection of a device, bond pads face down, onto a substrate with a matching array of bond pads. It offers several advantages, higher number of interconnects per unit area, smaller footprint, and faster interconnection speeds for example [2]. In comparison to wire bonding the technology is relatively immature, although advantages from flip chip assembly have resulted in significant growth in the number of flip chip devices in recent years [1]. Gallium arsenide devices however are further behind in the development of advanced packaging techniques in comparison to their silicon counterparts. As RF front-end modules develop with advancing architectures and increased functionally there is a constant constraint to reduce assembly cost and module footprint. Developing GaAs devices with flip chip capability is believed within Filtronic to be an attractive solution; chip attach methods will also reduce the module footprint. Lead based solders are commonly used in flip chip applications, however environmental awareness is becoming an area of growing importance in the electronics industry and manufacturers must be prepared to comply with international environmental policies [3]. Pb is a harmful environmental pollutant. Using Pb in electronic products is an increasingly visible environmental and political concern. OEM initiatives and legislation (such as RoHS and WEEE) are being implemented globally to drive the removal of Pb and other harmful materials from electronic products. These restrictions were taken into account when embarking on the flip chip process development cycle.

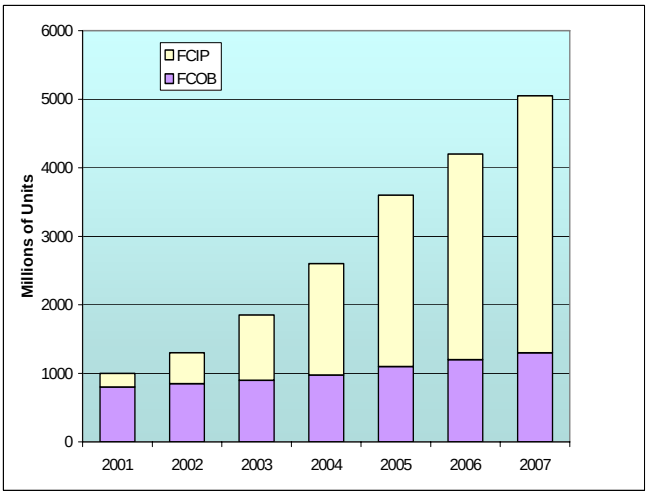

Figure 1. Increasing trend in flip chip production [1]

WAFER LEVEL PROCESSING

There are a variety of techniques for lead free solder bumping at a wafer level, choosing the optimal solder bump technique is a complex task heavily influenced by the requirements of the customer. Two parallel solder bump solutions have been pursued at Filtronic, electroplated solder deposition and laser dispense solder application. This paper will focus on the laser dispense process development.

The first stage of the process development requires design rules to be applied that accommodate the solder bump

process limitations. As a result minimum bond pad pitch and optimal passivation designs were evaluated. At the design stage consideration had to be given to the method of die separation. Typically scribe and break technology is utilized for the high volume switch line at Newton Aycliffe. This technology however is not compatible with solder bumped processing, for instance the die size to substrate thickness ratio necessitates the use of the break bar, which would damage the solder balls on the bond pads. Saw and laser dice however are alternative solutions, which need to be considered at the design stage. As reduced die size and increased chip count per wafer are key factors, this is a critical decision point and will be discussed later in more detail.

Implementing a solder bumped solution that would fit well with the existing manufacturing flow was the main influence on the choice of solder bump technology. Firstly the chosen method enables solder bumping of a pre-thinned GaAs wafer. One area of yield concern is in the thinning of solder bumped wafers post bump application. This can be restrictive to the final substrate thickness as well as being of concern for mechanical wafer yield. Additional stress induced during the thinning process may, for example, damage the passivation layer, presenting a potential concern for reliability. Therefore having the option to thin the wafer to the required thickness prior to solder ball application is felt to be a significant advantage.

Traditional interconnects for flip chip technology has been high lead and eutectic tin lead (SnPb) solders [2]. Further to directive 2002/95/EC on the Restriction of certain Hazardous Substances (RoHS) and Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE), which came into effect in July 2006, a commercially available solder process of lead free SnCuAg was the process of preference for Filtronic. SnCuAg and SnCu have demonstrated properties that are comparable to lead bearing solders [3].

An electro less plated barrier layer, also called the under bump metal (UBM), is selectively plated onto the bond pad opening, the main purpose of the UBM is to prevent diffusion of the Au into the Sn bond while also influencing the size and shape of the final bump by acting as a wettable material onto which the solder is applied. The integrity of this barrier is critical, as a defective barrier will allow the Au from the bond pad to diffuse into the Sn. Such a process failure would be a yield loss concern for the customer during the die attach process, at which stage the parts may be reflowed several times at temperatures around 250 degrees.

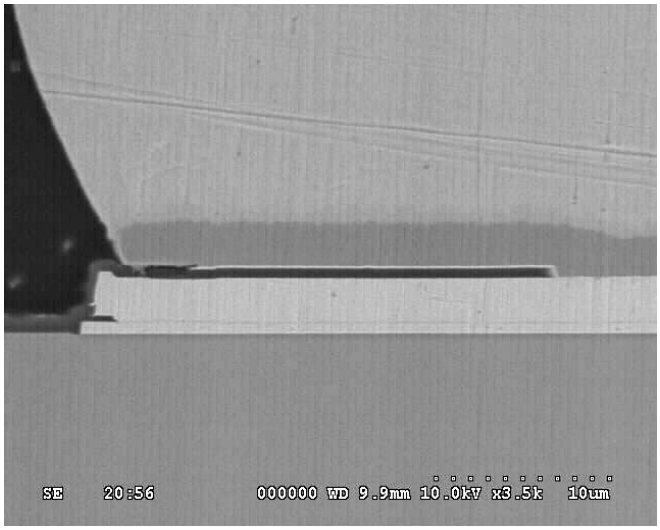

Figure 2. Image of solder and barrier layer, which prevents diffusion of the Au and Sn

After the UBM processing, pre-formed solder bumps are individually placed at speeds in excess of 10 balls per second. Gang ball placement methods are also emerging where all bond pads on the wafer are populated with solder balls in one step using a wafer level template. In the case of the individual ball jetting process laser melts the solder ball in a capillary, the molten solder is then ejected onto a wettable UBM material on top of the bond pad. Process critical monitors of the solder bump process include shear testing to verify adhesion, measurement of bump height and uniformity, inspection for surface defects and x-ray inspection of the solder ball and joint to verify there are no voids in the metallization.

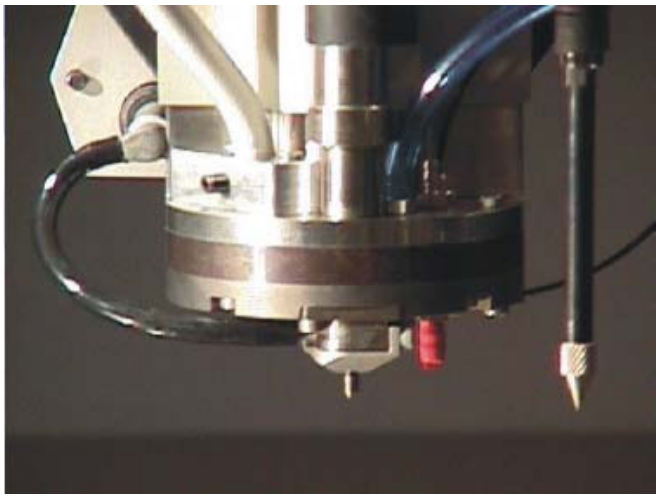

Figure 3. Laser dispense system for individual solder ball placement.

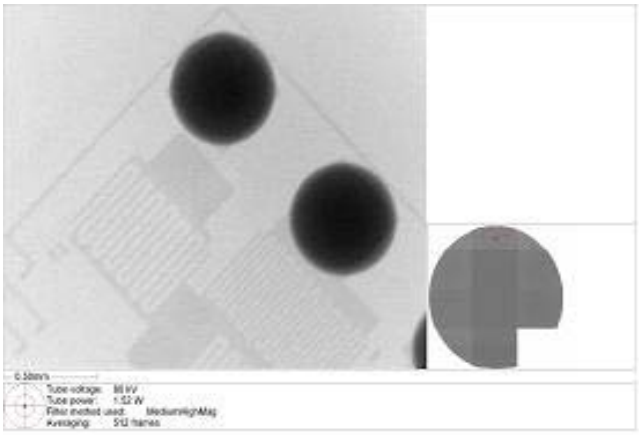

Figure 4. X-Ray analysis of individually placed solder balls.

Component level validation of the solder bump switch within Filtronic is ongoing. The test plan includes unbiased highly accelerated stress test (HAST), temperature cycling, and moisture sensitivity testing (MSL). Additional qualification of the part in package is ongoing with customers. The variety of substrates and under fills used in practice make it difficult to address all the possible options internally. Therefore working together with the customers through the qualification cycle is recognized to be best practice. Again environmental testing of the module is being conducted as well as shock and vibration tests.

PRODUCT TESTING

Depending on the product specification required by the customer, 100% product tested wafers might be required. This can be carried out easily with a pyramid probe. Product test yields on bump have been demonstrated to be equivalent to the yield achieved on an un-bumped wafer. Product test is preferentially carried out post bumping although a reflow may be requested to remove the resulting indentation in the solder.

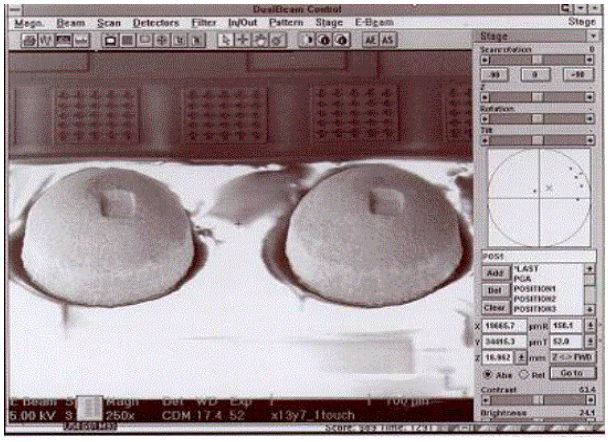

Figure 5. Product testing on solder bump utilising a cascade pyramid probe.

DIE SEPARATION

Singulation of die from a solder bumped wafer requires consideration at an early stage in the design cycle. Scribe and break, which is the standard method of singulation at FCSL, is not compatible with the development of a solder bumped route. The aspect ratio for example between substrate thickness and die size necessitates the use of the anvil break bar during the singulation process which would damage the solder bumps. This is an instant roadblock that requires an alternative dice technique to be pursued. Wafer saw and laser dice have been investigated as part of the process development cycle. At lower volumes, wafer saw is the cheapest and more readily available solution. Saw dice time for a typical 1mm sq production mask set is in the region of 12 hours, coupled with the requirement for an increased street width; saw can be somewhat more restrictive than the alternatives if high volume production is envisaged. A multi beam laser dice technology has demonstrated a fifteen times reduction in time to singulation, which is more suited to a high volume production environment. Utilising laser dice also gives the ability to reduce the street width; a reduction of 50% over typical street widths has been demonstrated. This leads to potential increases in the number of die per wafer of greater than 10%. The net advantages quickly reduce the cost of ownership. An additional advantage with multi beam laser technology is that the tool can be used interchangeably with all product lines at Newton Aycliffe due to the minimal kerf width required for laser dice. Saw on the other hand would be restricted to the solder bumped route as a result of the larger street requirement.

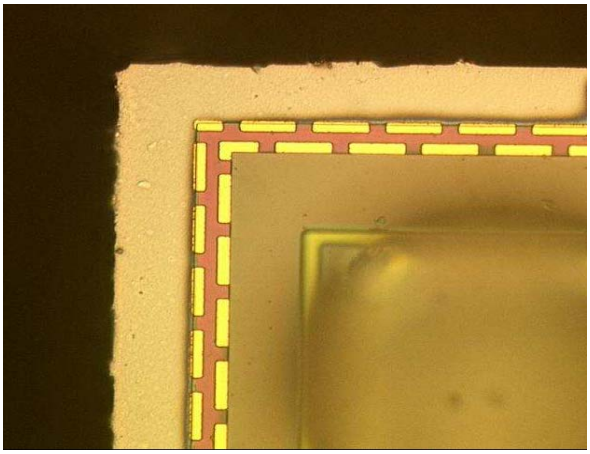

Figure 6. Laser dice of a solder bumped part demonstrated minimal kerf width and significantly reduced dice times. Courtesy of ALSI.

DIE SHIPMENT

Tape and Reel of bare solder bumped die is a practical method of handling and shipping die to ensure protection of the die and solder bumps while in transit.

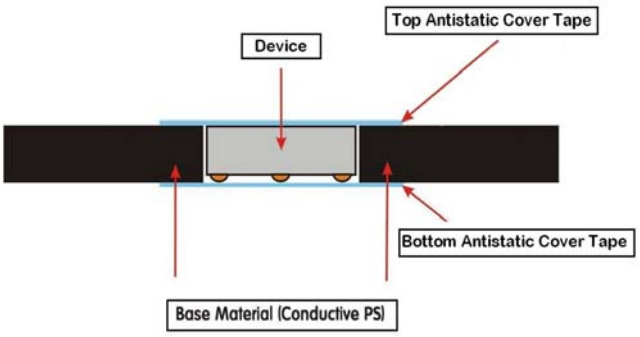

Figure 7. Illustration of a solder bumped die packaged in MicroTape tape and reel format.

Tape and reel of flip chip die is possible on machines such as the Isort by ASTI. As this is the final stage in the process flow prior to product being shipped to the customer, the Isort has an intelligent vision system, which enables top and bottom side inspection of the singulated die. The machine is also capable of inspecting for defects such as missing and damaged solder balls also cracked or chipped die. The die are then protected in the pocket of the customised MicroTape, which ensures the quality of the product once shipped to the customer.

CONCLUSION

To accommodate front-end module makers who are trending towards more advanced packaging solutions, which accommodate the increased pin counts of advancing architectures while also enabling simplified module assembly processes. Filtronic Compound Semiconductors' 150mm gallium arsenide wafer fab in Newton Aycliffe is developing a high yielding RF switch process with lead free flip chip capability.

Pb is a harmful environmental pollutant. Using Pb in electronic products is an increasingly visible environmental and political concern. OEM initiatives and legislation (such as RoHS and WEEE) are being implemented globally to drive the removal of Pb and other harmful materials from electronic products.
Component level and module based qualification of the process is currently underway.

ACKNOWLEDGEMENTS

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