High Voltage GaAs pHEMT Technology for S-band High Power Amplifiers

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Abstract

High voltage GaAs pHEMT technology with field plated gates has been in development at TriQuint since 2000, resulting in three processes that deliver state of the art performance up to Ku-band. We report on an S-band optimized version that will soon be transferred to production. At 3.5 GHz, it delivers power output density of 2.1 W/mm and 64 % PAE at 28 V. This technology is optimal for designing high power MMICs at S-band and provides a competitive alternative to GaN and SiC devices especially when cost, reliability and maturity are considered.

INTRODUCTION

TriQuint Semiconductor has developed 3 gallium arsenide processes that utilize field plated gates for high voltage pHEMT operation. First, the 0.35 um PWRPHEMT process is in production and used for applications up to 18 GHz and 12 V drain bias. This process was modified and optimized for higher power at X-band (8-12 GHz). This high voltage version is called HV3X and delivers 2.0 W/mm and 55 % PAE at 10 GHz and 15 V drain bias. It is also in production. Third, the GaAs pHEMT process reported in this work, HV3S, was developed and optimized for higher drain bias operation at S-band where it delivers power output density of 2.1 W/mm and 64 % PAE at 28 V. HV3S targets ship borne radar and commercial basestation applications and can be operated up to 28 V with a cutoff frequency of 7 GHz. This is a lower risk and lower cost approach compared to GaN or SiC technologies for obtaining the high power, proven reliability and low cost that are needed today for insertion into next generation radars and commercial applications.

After defining the process, efforts shifted to improving the manufacturability of HV3S. The primary focus was to accelerate the transfer to production and manufacturability of HV3S so that it can be inserted in radars in the near term. By improving yield and reducing cycle time, the result will be a lower cost process. Extensive testing at all stages of fabrication ensures that the process is robust to 28 V operation. Multi temperature DC reliability tests indicate mean lifetimes that exceed one million hours at a channel temperature of 200 °C and RF reliability tests confirm the DC results.

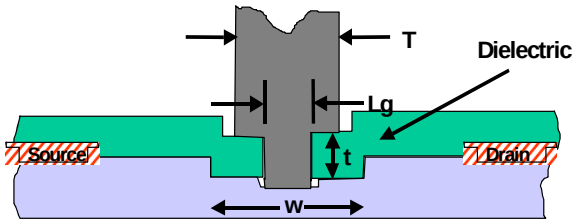

Figure 1. Channel parameters were optimized to increase operating voltage to 28 V.

PROCESS OPTIMIZATION

In order to operate at higher drain biases, the breakdown voltage has to be increased. This is accomplished at the expense of cutoff frequency. The optimal operating voltage increases with the size of the channel while the cutoff frequency decreases. In addition, operating voltage and power performance can be increased through the use of a field plate. Field plates were first employed in high voltage silicon devices [1] and have since been introduced effectively in GaAs [2,3,4] and GaN [5]. Recent reports of high voltage GaAs devices in the 26-28 V operating range [6,7,8] target high power applications in the commercial and military markets.

The HV3S process was developed for up to 28 V operation. Through on-wafer splits, channel parameters such as source-drain spacing, wide recess (w), field plate (T) and gate length size (Lg) as shown in Figure 1 were jointly optimized for best power and PAE at 24 and 28 V. In addition, robustness and survivability to over voltage spikes of up to 4 V were needed. The gate with integrated field plate is defined in two optical lithography steps as described in [9]. The trunk of the gate is defined in a thin dielectric layer that also provides an early passivation of surface states. The cap of the gate rests on the dielectric and acts as a field plate, reducing the high electric field at the base of the gate on the drain side. Electric field simulations and experimentation were used to determine the optimal dimensions. The device parameters of the HV3S process are shown in Table 1.

TABLE 1
DC PARAMETERS OF HV3S pHEMT PROCESS

Gm,max	250	mS/mm
Id,ss	180	mA/mm
Id,max	450	mA/mm
Vp	-1	V
BVds	78	V
Ron	3.8	Ω-mm

The epitaxial layer structure had to be modified to reduce buffer leakage at these high voltages. Buffer leakage can seriously degrade PAE in pHEMT structures operated at high voltages. Figure 2 plots the power output density and PAE as a function of drain bias for a typical 4x250 µm device tuned for maximum efficiency at 3.5 GHz. As shown, the peak in performance is at 32 V and the device survives up to 40 V. At 28 V, the device delivers 2.1 W/mm of output power, 64 % PAE and 14 dB of gain for an efficiency tune. Pout is quoted at the peak of the PAE which is similar to P1dB. Uniformity of the load pull measurements is very good with standard deviations of Pout and PAE both less than 5 %. The high PAE and power gain are essential to getting high power MMIC performance while maintaining reasonable power dissipation.

Over-voltage testing is done in three different ways to ensure robustness to the recommended operating voltage under different conditions: load pull, on-wafer RF probe and fixtured MMIC testing. Load pull is done under CW conditions until device failure. The MMICs are pulse tested in on-wafer and fixtured form up to 36 V.

PRODUCIBILITY

Having demonstrated excellent S-band performance at 24 and 28 V, our focus shifted to reducing cycle time and improving RF yields. Experiments were run to improve the manufacturability of the process. For example, the larger

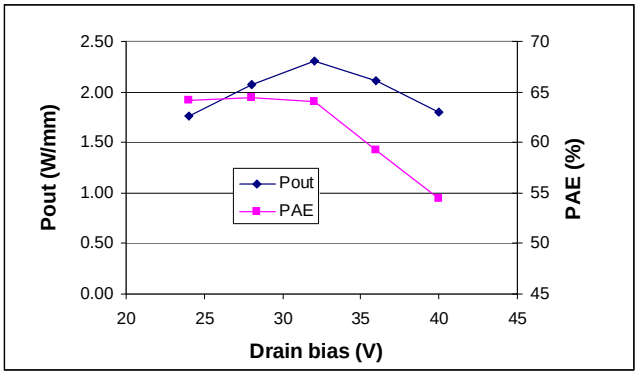

Figure 2. Efficiency tuned load pull at 3.5 GHz showing 2.3 W/mm and 65 % PAE at 32 V and device surviving up to 40 V.

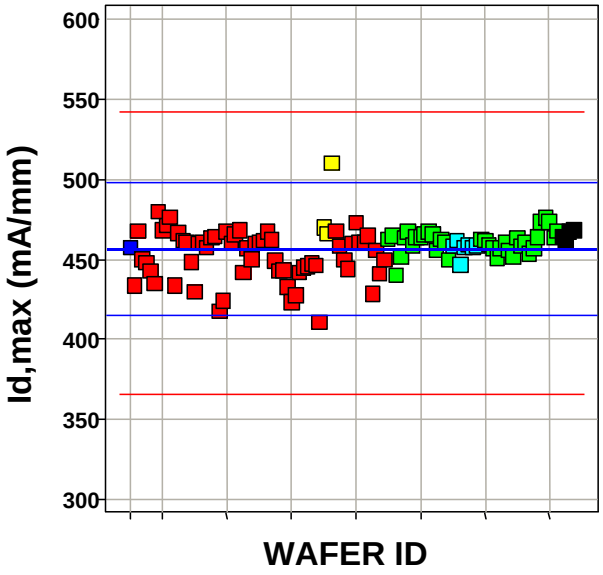

Figure 3. Trend chart of Id,max showing good process control and a Cpk of 2.0.

channel geometries enable less reliance on time consuming SEM measurements and are easier to control in general than our tighter geometry processes. Optimization of the new process steps from a manufacturing standpoint and a higher volume of wafers have also improved cycle time. The cycle time has dropped steadily in the past year and has already been reduced about 45 %.

In addition, the starting particle defect density must be tightly controlled to allow for very large capacitors that can not tolerate large defect densities. This problem is reliably screened out at DC or RF probe but was a significant yield loss when the program began. A reduction in starting particle density of 40 % has largely eliminated the yield loss due to failing capacitors. Sensitivity experiments of critical lithography steps ensured that process limits are set correctly for optimal throughput and performance. Data is collected from PCM structures during processing and from test structures and MMICs at both DC and RF probe. Statistical process control methodology is used to ensure that we have a stable and well controlled process. Figure 3 shows a trend chart of Id,max showing good control and a Cpk of 2.0.

Process stability is tracked using in-process and post-process data collection. Every MMIC is on-wafer RF tested and load pull data are taken on every wafer processed. The output power of both MMICs and discretes are all tightly distributed with standard deviations less than 0.2 dB. The yield of very large MMICs is now at the level of our established process technologies.

The baseline process will be released to production in Q1 2007 and will be available for foundry customers. Additional manufacturability improvements will be implemented and released to production later this year as they are proven out.

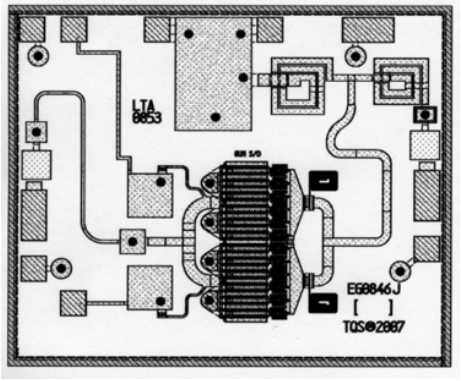

Figure 4. Layout of the 4.8 mm gate periphery one-stage MMIC used for process monitoring and reliability testing. Die size is 1.8 x2.1 mm^2.

These will further improve yield and cycle time while maintaining the same performance.

MMIC DESIGN

S-band high power amplifier MMICs designed in this process have demonstrated high power and high PAE at S-band at drain voltages of 24 to 28 V. In addition, fixtured devices survived robustness testing to 36 V which is the limit of the pulse modulator that was used. Power density increased steadily with drain voltage.

A smaller S-band MMIC (Figure 4) was designed for process monitoring and reliability testing. Die size is 1.8 x 2.1 mm^2 and it has 4.8 mm of gate periphery. This mini amplifier was designed to deliver a fixed amount of power instead of maximum PAE. At 24 V it has 7 to 8 watts of power from 2.6 to 3.4 GHz for a power output density of up to 1.7 W/mm and PAE ranges from 45 to 51 % (Figure 5). At 32 V, the power output density is over 2 W/mm, consistent with the load pull measurements of the 1mm devices. Devices also survived to 36 V with no failures.

RELIABILITY

Extensive reliability testing has been performed from 24 to

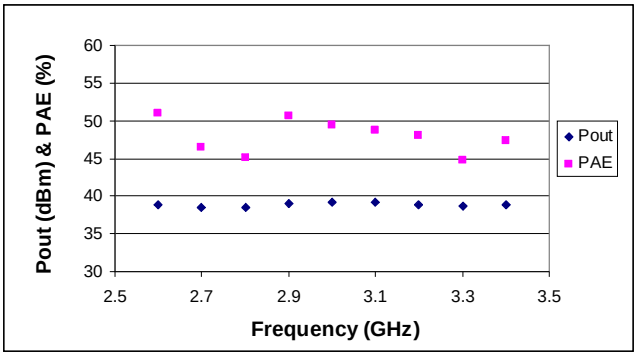

Figure 5. Power output and PAE of the 2.1x1.8 mm^2 process monitor/reliability MMIC.

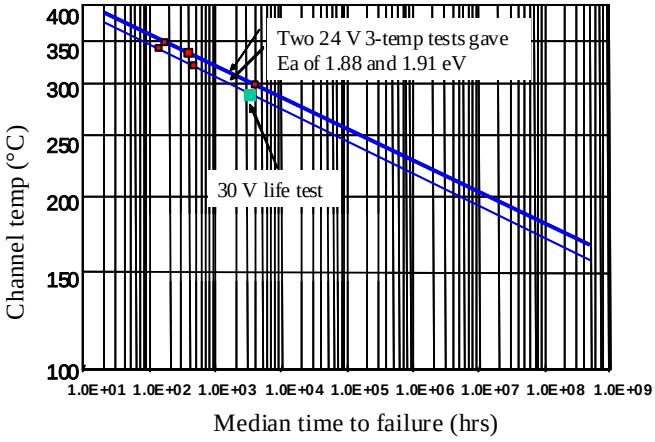

Figure 6. Multi-temperature DC lifetests showing activation energy of ~ 1.9 eV and 5e6 hours lifetime at 200 °C. A 30 V single temperature test lies on one of the 24 V lines.

30 V on the HV3S process. Multi-temperature DC life tests indicate an activation energy of 1.9 eV and an MTTF of at least 5 million hours at a channel temperature of 200 °C (Figure 6). Eighty four devices from 2 lots separated in time by 8 months were used. The lowest temperature test lasted over 8 months. A suitably low temperature was chosen to look for non-thermally activated failures that can be masked when only testing at high temperatures. In addition, passive components have been tested to higher voltages to ensure their reliability under higher voltage operation.

RF life tests of HV3S MMICs confirmed the lifetime and activation energy that were found in the DC life tests. The single stage, 50 ohm matched, reliability MMIC was used for these tests. This makes it easier to calculate the peak channel temperature. It also eliminates questions of inter stage matching that can complicate multi stage RF life tests while still exercising the active and passive MMIC elements with RF energy. A failure criteria of 10% change in drain current was used which corresponds to a drop in output power of approximately 0.5 dB. An activation energy of 2.0 eV for the three temperature RF test was calculated. The predicted lifetime at 200 °C channel temperature exceeds 1e7 hours and the lower bound of the 90% confidence level is 5 million hours.

Convinced that thermally activated degradation was not going to be a significant determinant of device lifetime, we are now looking into voltage accelerated mechanisms. Since most GaAs devices have operated around 10 V or less, there was a concern that new failure mechanisms might be introduced at these higher voltages. An RF life test at 3 voltages will be started. The voltages are 24, 27 and 30 V and the channel temperature will be held under 250 °C. This will eliminate thermal degradation as little to no thermally activated degradation is expected to be seen at this channel temperature. The behavior of the different voltages will be compared with one another to determine if there is a voltage

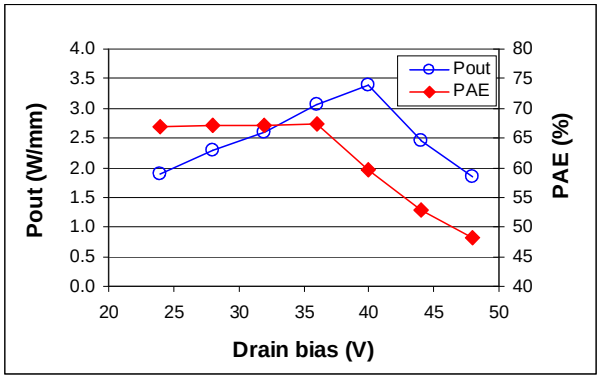

Figure 7. An advanced process is in development for higher voltage and power output. Preliminary results are 3.4 W/mm and 60 % PAE at 40 V of drain bias.

accelerant. Voltages over 30 V can be explored when our new reliability test equipment is installed. We already have one data point at 30 V from a DC life test. As shown in Figure 6, this point lies right in line with the 24 V data points so we are not expecting to see a voltage accelerant.

ADVANCED PROCESS

A higher voltage process is in development for up to 40 V S-band applications. As shown in Figure 7, a result of 3.4 W/mm (3.6 W/mm saturated) and 60 % PAE has already been achieved at 40 V drain bias on a 4x250 µm device. This represents the highest reported power output density for a GaAs device. These devices survived to 48 V before failure. Thermal management will become crucial at these high power densities and will be essential to maintaining reasonable channel temperatures and performance. These voltage and power levels are competitive with GaN and SiC technologies and offer a lower cost and potentially lower risk approach to high power at S-band.

CONCLUSION

A 28 V GaAs pHEMT process has been developed for S-band operation. It offers high power output density, gain and PAE and is suitable for high power S-band applications. The manufacturability of this process has been improved, resulting in lower cycle time and higher yields. DC and RF reliability tests indicate a mean time to failure of over one million hours at a channel temperature of 200 °C. An advanced process is being developed for even higher power applications operated at 40 V.

ACKNOWLEDGEMENTS

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ACRONYMS

GaAs: Gallium Arsenide
GaN: Gallium Nitride
MMIC: Monolithic Microwave Integrated Circuit
MTTF: Mean Time To Failure
NRL: Naval Research Laboratory
ONR: Office of Naval Research
PAE: Power Added Efficiency
PCM: Process Control Monitor
pHEMT: pseudomorphic High Electron Mobility Transistor
SEM: Scanning Electron Microscope
SiC: Silicon Carbide