pHEMT Gate Formation Using a Dielectrically Defined Gate with No Plasma Damage

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Abstract

A pHEMT gate formation process using a dielectrically defined gate window with no plasma damage to the gate layer has been developed. The process is compatible with field plates of arbitrarily large dimensions and is extendable to a reduced gate length through the use of a dielectric spacer process.

INTRODUCTION

A pHEMT process that provides for maximum protection of sensitive substrate layers has been developed. This type of process is desirable because of improved manufacturability as compared to those that permit plasma or chemical damage to sensitive pHEMT substrates. A double recessed process with dielectrically defined gates that meets this requirement has been achieved through passivation of the substrates with a protective film very early in the build sequence. This protective film remains in place during any potentially damaging plasma [1] or chemical exposure and is removed just prior to gate formation. The process developed is easily extended to critical dimensions beyond the capability of standard lithographic techniques through the use of a dielectric spacer [2] – which has been demonstrated, and is fully compatible with field plate formation for higher voltage devices. Any field plate structures utilized may be arbitrarily large in contrast with the limitations of a traditional T-gate approach.

Considerations of the desired device, the substrates used, and the equipment set provided the direction for the process definition. A process that could provide small uniform gate critical dimensions without plasma damage to the substrates was sought. In order to accomplish this, the epitaxial substrates designed to produce the desired transistor characteristics were passivated as early as possible in the process flow. Potentially damaging chemical or energetic plasma processing was executed only with protective films in place over the device areas. The starting material was designed with two etch stop layers to accurately control the depth of both recess layers. A PECVD passivation layer is deposited immediately after the first recess etch (first wafer fabrication layer). This layer is then masked and etched to define the gate windows through which a clearing etch, the second recess and gate metal deposition processes are to be carried out.

Gate window formation for this process utilizes an interferometrically controlled partial PERIE dry etch followed by a wet clearing etch later in the process flow. Plasma damage to sensitive epitaxial layers is avoided by termination of the PERIE etch with a well controlled thickness of dielectric remaining on the gate layer. Determination of the minimum required dielectric thickness to protect the gate layer was accomplished by monitoring substrate conductance as a function of remaining dielectric thickness after plasma etching. An optical signal from the reactive plasma is used to monitor and terminate the dry etch. Gate formation is completed by clearing the remaining nitride with a wet HF etch, followed by photo patterning for the gate metal, a recess etch, and deposition of gate metal employing a lift-off technique.

This process offers advantages over other published methods [1], [3] in that it utilizes a single homogenous dielectric film and relatively simple etch equipment and methods to define the gate windows. It uses a hybrid process for gate definition and is unique in its application of a specialized optical endpoint detection technique to control the dry etch.

PLASMA DAMAGE EVALUATION

The overall process was developed with the intent of minimizing damage to the epitaxial layers on the starting material in order to produce pHEMT devices with characteristics that are not compromised by exposure to plasma or chemical damage during wafer processing. This is accomplished by preventing contact with potentially damaging chemicals and establishing the minimum protective film thickness required to prevent plasma damage. A continuous film impervious to chemical attack covering the FET area on the wafer is sufficient to fulfill the chemical exposure requirement. In order to evaluate plasma damage prevention, however, a reliable test methodology was needed. Sheet conductance measurements were used to characterize plasma damage.

Conductance measurements were made on pHEMT substrates subjected to representative processing steps in

several experiments. These measurements were made on a Lehighton LEI Model 1310 Contactless Measurement System. Experiment 1 was devised to test the effects of the then standard processing (low damage dry clearing) and a "downstream" clearing as a potential improvement on the $Al_xGa_{1-x}As$ Schottky layer. Experiment 2 evaluated the effects of subsequent processing on substrates processed through first recess. Experiment 3 was conducted as a supplement to Experiment 2 in order to provide data on substrates more representative of the planned process.

Typical pHEMT epi wafers were used for Experiment 1. Initial conductance measurements were made on two wafers etched to the Schottky layer. The wet etch was repeated on half of the first wafer (designated "2 crown" in Figure 1) to confirm etch completion. Measurements were made after one hour of wait time to assess stability of the substrates (displayed as "3 1 hour" in Figure 1). The first wafer was then measured after each of the following: 20 seconds of the "low damage" dry clearing etch; a repeat of that etch; two hours of exposure to lab ambient; chemical strip in NMP; repeat of the chemical strip; exposure to the resist develop process; overnight wait; and an ohmic contact alloy cycle. Figure 1 is a plot of the conductance measurements with the experimental treatment (sequentially numbered) shown on the x-axis. The data indicate that the dry clearing etch (noted as "4 20 et" and "5 2nd 20" in Figure 3) thought to be a "low damage" etch caused a significant reduction in the film conductance as compared to the baseline value indicated by the first three x categorical values in Figure 1. Other processing investigated produced little or no degradation in the conductance values.

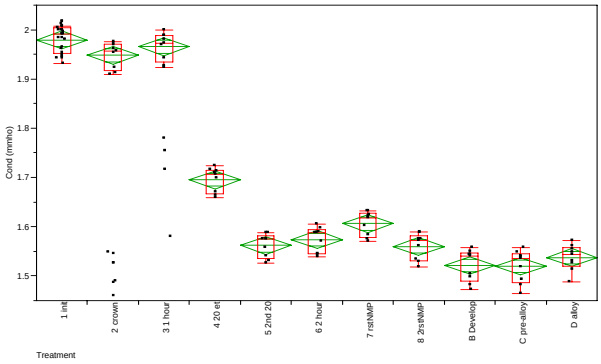

Fig 1. Plot of conductance measurements as a function of experimental treatment of pHEMT substrate with Schottky layer exposed.

The second wafer in this experiment evaluated a "downstream" clearing etch step, i.e. an etch with no RF power applied to the lower electrode in the etch tool and repeated the "low damage" treatment of wafer one as a control. Figure 2 shows the results of the conductance measurements on the second wafer in the first experiment. Again, the plasma processing thought to be low or no damage caused a loss of conductance indicative of damage to the epitaxial layers on the substrate, but may be limited in extent as indicated by little or no additional damage by the second "downstream" etch. This experiment proved to be a sensitive gauge of process induced damage and demonstrated that plasma etch of the gate windows to completion with the tools evaluated would damage exposed epitaxial layers.

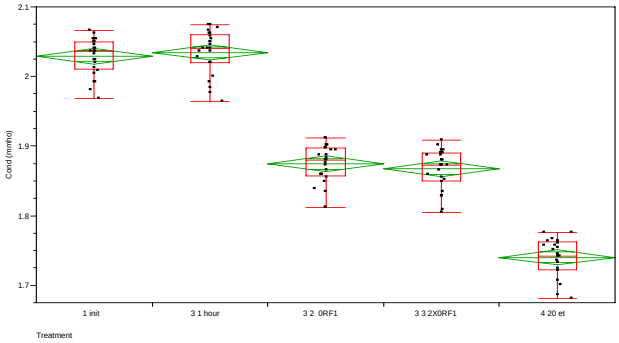

Fig 2. Plot of conductance measurements as a function of experimental treatment of pHEMT substrate with Schottky layer exposed.

Experiment 2 sought to establish gate etch process limitations using substrates more representative of the planned product. This sample had a 100 Å thick doped GaAs cap layer between the first and second etch stop. In the device process this layer is exposed at first recess, passivated with PECVD nitride, and is left in place atop the Gate layer until after the gate window is defined, thereby providing some shielding for the Gate layer. The thickness of this layer on this evaluation wafer was less than any anticipated in production material and should have been more sensitive to damage to the $Al_xGa_{1-x}As$ Schottky layer than planned product. Though not as sensitive as the wafers used in the first experiment, it should provide a realistic evaluation vehicle for production processing.

This second experiment was designed to determine the minimum remaining dielectric film thickness needed to prevent plasma damage. The wafer was wet etched through the first recess process, including removal of the first stop layer and measured. The wafer was then processed and measured after each of the following: PECVD deposition of 3000 Å of silicon nitride; photo processing to mask half of the wafer to serve as a control; plasma etch of the nitride to 780 Å remaining thickness; plasma etch to 624 Å remaining; plasma etch to 460 Å remaining; plasma resist strip in the same etch tool, resulting in 390 Å remaining nitride; plasma etch to 240 Å remaining nitride; a 2.5 minute HF etch to remove remaining nitride on the experimental half of the wafer; additional HF etch to remove nitride on the control half of the wafer; and second recess etch. Figure 3 indicates the results of the measurements after each of these processing steps. Symbols used in the plot are indicative of the measurements as being from masked, open, or border between masked and open areas on the wafer. Uncertainty in manual placement of the wafers on the Lehighton necessitated the exclusion of the border region from the data analysis because of the inability to determine whether the

measured value was from a masked, unmasked, or partially masked area. Plasma damage was apparent after etching the dielectric to 240 Å. At this point the nitride was wet etched in two steps – the first to remove the nitride on the evaluation half of the wafer and the second to complete the removal of the nitride on the control half of the wafer. Next, the wafer was recess etched to the Schottky layer. The difference between the control half and the evaluation half of the wafer in the final measurements indicate that damage to the Gate layer had occurred through the remaining nitride, cap, and stop layers.

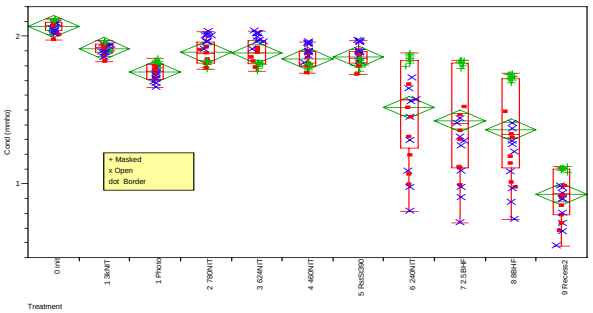

Fig 3. Plot of conductance measurements as a function of experimental treatment of pHEMT substrate in Experiment 2

Experiment 3 explored the response of substrates truly representative of planned production. This experiment was essentially a repeat of Experiment 2 using a 400 Å doped GaAs cap layer between the two etch stop layers. Figure 4 depicts the results from this testing and shows that this plasma processing may be used to a remaining nitride thickness of 220 Å. A minimum remaining nitride thickness of 300 Å and an etch process to minimize variation of the same has been established for production. This experiment included a wet clean (denoted 6 EG240) after the plasma resist strip to represent actual processing.

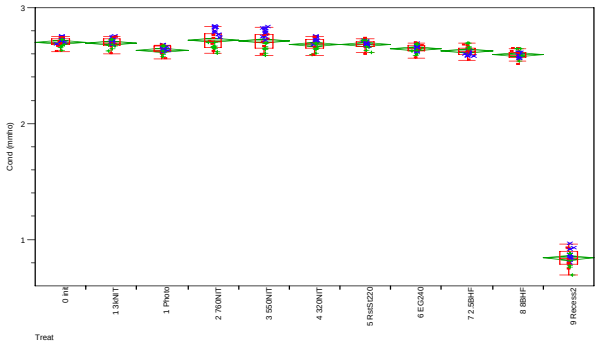

Fig 4 Plot of conductance measurements as a function of experimental treatment of pHEMT substrate in Experiment 3.

GATE PROCESSING

The initial process evaluation included various process flows and a gate window definition that included all dry etching. Flow variants were primarily focused on the placement of the ohmic contact and isolation implant processing and whether or not a dielectric spacer was used. The isolation implant proved to severely degrade the uniformity of the gate window dry etch and, therefore, was performed after the dry gate window etching. Additionally, the "no damage" dry etch step caused degradation of the substrate material if carried out to completion and was abandoned in favor of a partial dry etch followed by a wet clearing etch. An HCl solution was used for removal of stop layers and GaAs cap layers were etched using either an $NH_4OH:H_2O_2$ or an $H_2SO_4:H_2O_2$ solution. A stop layer in combination with the passivation layer enables the process to accommodate a second recess over etch to produce a region outside of the gate window opening that is confined between the passivation layer and the stop with the lateral extension of the recess determined by the etch time. The resulting structure is shown in the completed device as the dark areas on either side of the gate metal in Figure 6. This "ungated" or "vacuum passivated" recess [4] is used in conjunction with the epitaxial layer parameters to provide the desired electrical characteristics.

The gate formation for this process is initiated by defining the gate locations in a photoresist masked dielectric layer on pHEMT substrates. After patterning using a RELACS™ enhanced photolithography process, the gate dielectric is etched in a Trikon (now Aviza) Omega 201™ PERIE etch system. This etch is controlled by an interferometric technique and leaves a well controlled thickness of dielectric in place in the gate windows to protect the underlying epitaxial layers from chemical and plasma exposure that follows. An optional sidewall spacer process may be executed at this point. The spacer processing consists of the deposition and anisotropic dry etch of a second PECVD layer utilizing the same etch control methodology. The purpose of the spacer process is to reduce the gate critical dimension. Figure 5 shows a monochromatically selected wavelength optical intensity signal from the RIE plasma. The periodic form of the signal is caused by detection of direct and substrate reflected radiation.

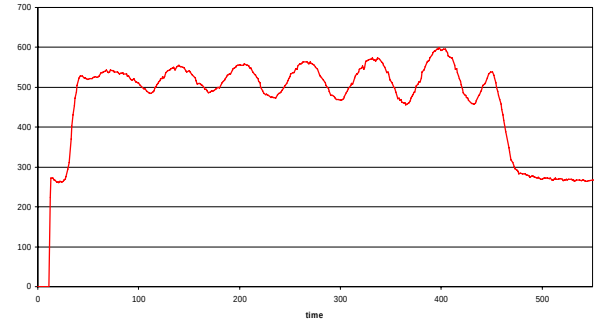

Fig 5. Optical intensity signal from etch of silicon nitride film in Omega etcher.

After gate window dry etch, processing is continued through device isolation, ohmic contact formation and any other steps desired prior to Schottky gate formation. Just prior to gate metal processing, the remaining nitride in the gate windows is cleared with a wet etch. A resist lift-off pattern is then used to define a gate metal layer. A second wet recess etch to a stop layer is executed with this resist pattern in place. Metal evaporation and lift-off complete the gate formation process. The resulting structure (see Figure 6) is a T-gate with the stem dimension established by the dielectric opening, the width of the T top defined by the resist opening and the length of the "ungated recess" determined by the second recess over etch.

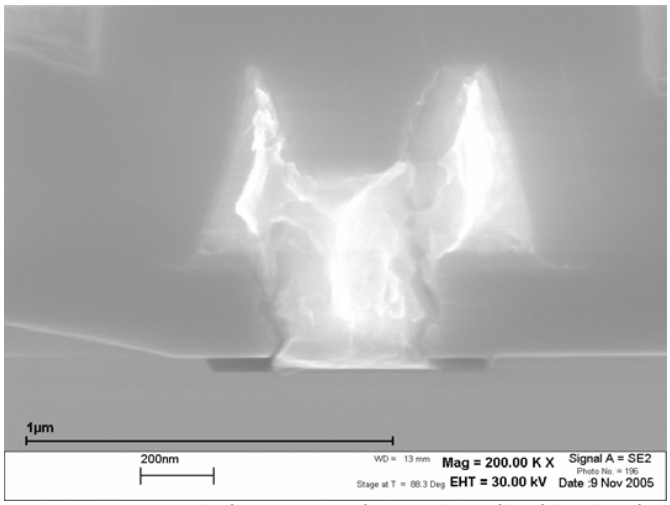

Fig 6. SEM micrograph of cross section of FET. The profile of the edge of the first recess may be seen on the left side of the micrograph.

CONCLUSIONS

A gate formation process for a versatile double recessed pHEMT process with no plasma damage has been developed using dielectrically defined gate windows. A novel evaluation technique with intentionally varying sensitivity to assess damage to pHEMT substrates was employed to determine process limitations. These limitations combined with other desired characteristics such a minimal gate critical dimension imposed stringent limitations on the gate window definition. In order to comply with these restrictions, the gate window plasma etch needed to be terminated with a precisely controlled thin layer of dielectric remaining in the gate windows to prevent plasma or chemical damage. A control technique for the plasma etch was constructed using the reactive plasma discharge as a source for an optical interference signal used to monitor and terminate the etch. The process is extendable to small gate critical dimensions through a dielectric spacer process with appropriately chosen parameters and is compatible with very flexible field plate processing.

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NOTES

RELACS is a trademark of AZ Electronic Materials USA Corp.
Omega 201 is a trademark of Aviza Corp.
JMP is a trademark of The SAS Institute

REFERENCES

[1] M. Martinez, E. Schrimann, M. Durlam, D. Halchin, R. Burton, J.-H. Haung, S. Tehrani, A. Reyes, D. Green, N. Cody, "P-HEMTS for Low Voltage Portable Applications Using Filled Gate Fabrication Process," *GaAs IC Symposium Technical Digest*, pp. 241-244, 1996

[2] H. Siweris, A. Werthof, H. Tischer, U. Schaper, A. Schafer, L. Verweyen, T. Grave, G. Bock, M. Schlechtweg, W. Kellner, "Low-cost GaAs pHEMT MMIC's for millimeter-wave sensor applications," *IEEE Transactions on Microwave Theory and Techniques*, Volume 46, Issue 12, Part 2, pp. 2560-2567, Dec. 1998

[3] D. Fanning, L. Witkowski, J. Stidham, H.-Q. Tserng, M. Muir, and P. Saunier, "Dielectrically Defined Optical T-gate for High Power GaAs pHEMTs," *2002 GaAs MANTECH Digest of Papers*, pp. 83-86, 2002

[4] D. Atwood, "Vacuum Passivated T-gates: A New Method for Fabricating Submicron Gates," *Proc. SPIE* , 1263, pp. 209-216, Mar. 1990

ACRONYMS

pHEMT: pseudomorphic High Electron Mobility Transistor
PERIE: Plasma Enhanced Reactive Ion Etch
PECVD: Plasma Enhanced Chemical Vapor Deposition
NMP: n-methyl pyrrolidone