Planarization Process for Transparent Polyimide Coatings to Reduce Topography and Overburden Variation

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Abstract

Surface topography and overburden variation are encountered during Gallium Arsenide (GaAs) device manufacturing processes and have a significant impact on device performance and yield. A planarization process, CON-TACT® planarization, is presented to locally and globally planarize GaAs heterojunction bipolar transistor (HBT) wafers coated with polyimide material. This planarization process involves physically forcing the flowable material from the raised into the recessed areas to create a planar surface. As a result, the surface topography and overburden variation are significantly reduced, and broader processing latitudes are secured for downstream processes. Consequently, easier process control, more consistent device performance, and higher yield can be achieved.

INTRODUCTION

GaAs devices, such as heterojunction bipolar transistors (HBTs) or pseudomorphic high electron mobility transistors (PHEMTs), have significant local topography, in addition to the typical die-to-die variation or global topography, due to the various epitaxial layer mesas, pedestals, trenches, and interconnection layers present. A GaAs HBT consists of the collector trench, the base pedestal, and the emitter mesa, which may have topography differences of 3 µm or larger. Because of their chemical, physical, electrical, and mechanical properties, polyimide films are often used as interlayer dielectrics (ILDs) and as stress buffer/passivation layers for many GaAs and other compound semiconductor technologies. However, polyimides lack a planarizing capability, which has made it challenging to successfully fabricate devices when multilayer ILDs and interconnects are desired or required.

Topography is introduced after the first layer of structures is fabricated on the substrate. As more layers of ILDs and interconnects are fabricated atop, the topography increases. In addition to increasing topography, variation in the overburden thickness (coating thickness on top of the structures) increases, which further worsens and increases the complexity of the fabrication processes. Although, applying a relatively thick coating can planarize sub-micron structures, topography and overburden variation over large structures remain problematic. Furthermore, applying a thick coating is not always desirable and adds or creates other concerns or problems. Therefore, topography and overburden variation obviously must be reduced for better process control and ultimately better yield. Although chemical mechanical planarization (CMP) has been proven for silicon semiconductor manufacturing to reduce the topography, it may be incompatible with compound semiconductor processing. Furthermore, it is extremely difficult for CMP to planarize polymeric material [1]. Therefore, an alternative planarization method is needed to planarize polymeric materials. A planarization process for reducing polyimide coating topography and overburden variation, CON-TACT® planarization, is introduced and reported here.

CON-TACT® PLANARIZATION TECHNOLOGY

CON-TACT® planarization technology has been used to planarize various materials for different applications [2-9]. It has proved to provide local and global planarization with very uniform thickness [4]. CON-TACT® planarization utilizes external force to bring an optically flat surface in contact with the coated, flowable planarization materials. The optically flat surface planarity is replicated to the flowable planarization material surface. The material is then hardened and separated from the optically flat surface. This planarization technology is a wafer-scale process that achieves local and global planarity simultaneously. There are two different types of CON-TACT® planarization processes. The first relies on photo-radiation to harden or cure the planarizing material, while the second is a thermal process that relies on manipulating the temperature to harden or cure the planarizing material [4, 9].

The general process flow of CON-TACT® planarization technology is illustrated in Figure 1. The process starts with a substrate that has a topographic surface with a planarization material deposited atop. The deposited planarization material tends to conform to the underlying topographic structures and produces significant surface topography, Figure 1(A). Under appropriate conditions, an anti-stick optically flat surface is brought into contact with the coated flowable planarization material, Figure 1(B). Sufficient pressure is then applied to physically force the material to flow from high to low surface topographic areas and conform to the optically flat surface,

Figure 1(C). Subsequently, the planarized flowable material is hardened or cured using either a photo-radiation or a thermal process, or both, depending on the material characteristics. Once the material is hardened, the anti-stick optically flat surface is separated from the material surface, Figure 1(D). This results in the replication of the optically flat surface planarity on the hardened planarized material surface with local and global planarization.

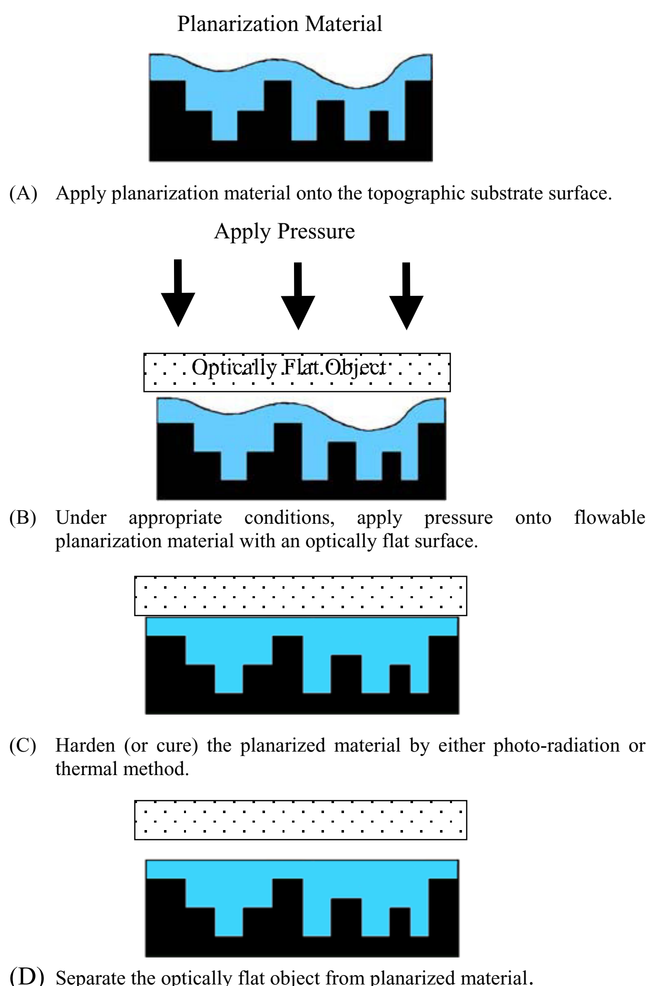

Figure 1. A representative process scheme of CON-TACT® planarization technology.

In this study, GaAs HBT device wafers were spin-coated with about 3.5 µm and 5.0 µm of Brewer Science's T-Polyim™ T-20020 polyimide. The HBT device wafer has topography ranging from 1.0 µm to 2.0 µm and structure sizes ranging from a few micrometers to more than 100 µm. These wafers were processed using the thermal CON-TACT® planarization process, which was developed based on the material's thermal characteristics. A coated device wafer fabricated with a process identical to the planarized wafers except without the planarization step, was prepared and used for comparison. This wafer was referred as the "reference" wafer and was made to ensure a more meaningful planarization performance comparison since both planarized and reference wafers experienced almost identical thermal history and process environments.

RESULTS AND DISCUSSIONS

A 2.25-µm thick T-20020 coating on a quartz wafer was characterized for its percent transmission using a Varian Cary 500 Scan UV-VIS-NIR dual beam spectrophotometer (Figure 2). Refractive index (*n*) and extinction coefficient (*k*) were measured using a J.A. Woollam M2000 variable-angle spectroscopic ellipsometer (M2000 VASE®) (Figure 3). These results indicate that T-20020 is very transparent in the visible wavelength range. As shown in Figure 3, the extinction coefficient, *k*, is very low even at 300 nm ($k \cong 0.055$) which is below the visible spectrum. This indicates that the film does not absorb light in the measured wavelength range, 300 to 1700 nm. In addition, this material has a relatively high refractive index (*n*) of about 1.68 to 1.78 in the wavelength range of 400 to 700 nm. Furthermore, the thermal stability of the cured T-20020 was characterized and showed good stability at temperatures higher than 400ºC. The glass transition temperature of the film measured was greater than 330ºC. These results indicate that the T-Polyim™ is suitable for use as passivation/packaging layers for certain light-emitting compound semiconductor devices, such as light-emitting diodes (LEDs), in addition to as interlevel dielectric layer.

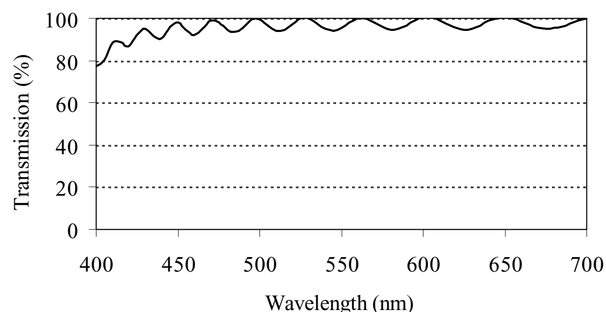

Figure 2. Percent transmission chart of a 2.25-µm T-20020 film on a quartz wafer.

Both reference and planarized wafer were characterized for planarization performance. The original device wafer topography was measured for comparison as well. A Dektak® 8 stylus profiler (From Veeco) was used to characterize the surface topography across the die. As shown in Figure 4, the topography (step height) was reduced from about 13,500 Å on the reference wafer to about 3,500 Å on the planarized wafer, after undergoing a required 100ºC bake for 2 minutes to further remove the residual solvent. The step height was about 2000 Å prior to the additional baking step.

These results show a ~75% reduction of topography with CON-TACT® planarization technology. Different locations within a die were characterized for surface topography with consistent results. Different dies across the wafer were characterized and resulted in very comparable surface topography for the planarization wafer.

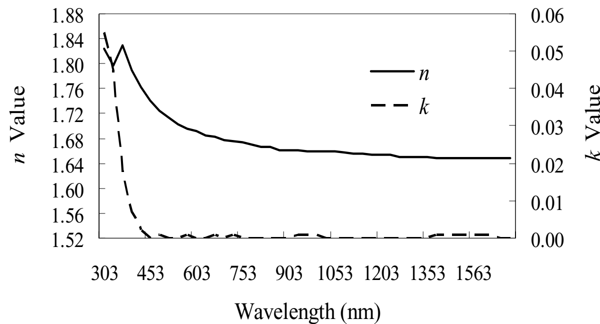

Figure 3. Refractive index (n) and extinction coefficient (k) for a T-20020 film.

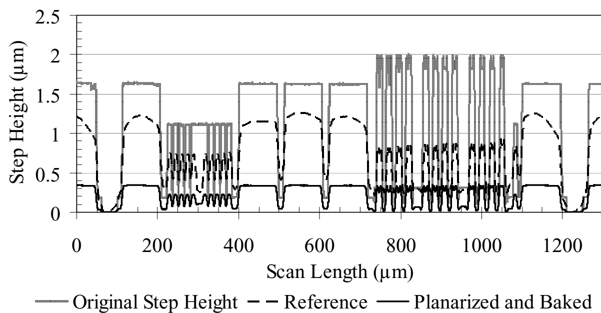

Figure 4. Cross-die step heights measured from the original device wafer, the reflowed reference wafer, and the planarized wafer after 100ºC bake. The thickness of the T-20020 was about 3.5 μm.

Cross-sectional micrographs of both reference and planarized wafers were taken using an FEI model 820 (from FEI) dual-beam focused ion beam scanning electron microscope (FIB/SEM). The thermal reflow process (reference) does provide some level of local planarization on top of smaller structures, such as HBT (Figure 5(A)). However, it is evident that local planarization has been improved with the application of CON-TACT® planarization (Figure 5(B)). The improvement is even more prominent when the planarity across large structures, such as bond pad and die street, was characterized. The planarized wafer has a much improved planarity with a step height of ~0.3-0.4 μm (Figure 6(A)), as opposed to a step height of ~1.2-1.3 μm for the reference wafer (Figure 6(B)). These findings indicated that the thermal reflow process smoothes the slope on the edge of the underlying topographic structures and normally provides local planarity for small topographic structures. As shown in Figures 4-6, using only the thermal reflow process is not capable of providing good planarity, especially for the large topographic structures. The planarized wafer showed much greater reduced topography and much better local and global planarity across both small and large topographic structures.

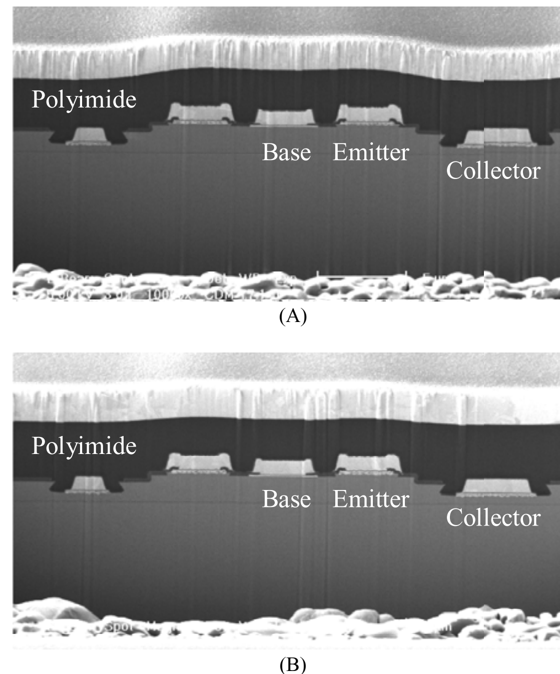

Figure 5. GaAs HBT cross-sectional FIB/SEM micrographs of (A) reference and (B) planarized wafers.

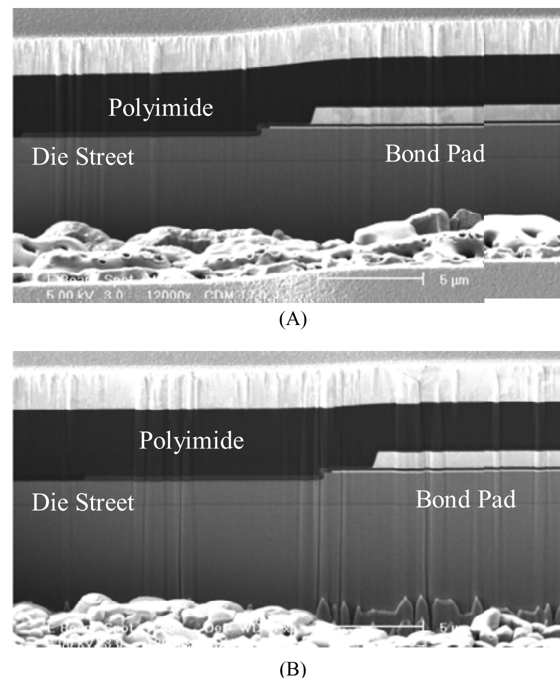

Figure 6. Cross-sectional FIB/SEM micrographs of (A) reference and (B) planarized wafers taken across the bond pad and die street regions.

The overburden thickness was measured using a NanoSpec® 6100 (Nanometrics Incorporated) film analysis system having a 25-µm measuring laser beam diameter. Film thicknesses on top of the bond pad structures within a die were measured. Five dies across the wafer were measured.

The overburden thicknesses on top of the bond pads within the die were measured. The overburden thickness variation was calculated (Figure 7). The overburden variation measured from the reference wafer was about 1000 Å and greater. This is primarily caused by the surrounding structure layout of the bond pads measured and the location of each bond pad within the die. Such a level of overburden thickness variation could severely affect the subsequent processes and could result in catastrophic device failure. Therefore, the variation needs to be reduced prior to further processing. With the application of the CON-TACT® planarization process, the overburden variation was reduced to as low as 100 Å or even lower. As such, an overburden thickness variation reduction of about 90% was accomplished.

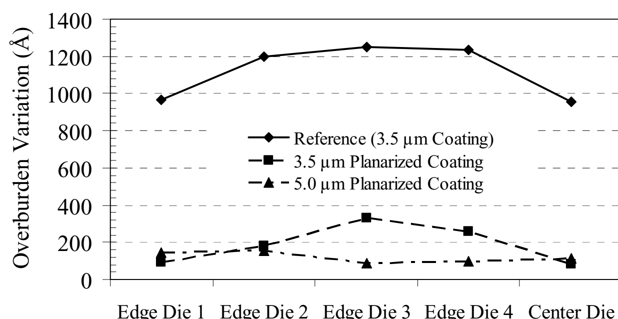

Figure 7. Within-die overburden variations measured from the reference and planarized wafers with overburden thicknesses of about 3.5 µm and 5.0 µm.

Conclusion

A polyimide, T-Polyim™, has been demonstrated to provide a highly transparent layer in the visible light wavelength range. CON-TACT® planarization technology has proven its capability of planarizing a ~3.5-µm-thick transparent polyimide coating on GaAs HBT structures of 2.0-µm topography with sizes ranging from a few microns to over 100 µm. A topography reduction of 75%, as compared to that of thermal reflow processing, has been achieved. Within die overburden variation was reduced for 90% or more. The reduction of topography and overburden variation provides better process control and will ultimately lead to higher yield.

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Acronyms

CMP: Chemical Mechanical Planarization
FIB/SEM: Focused Ion Beam Scanning Electron Microscope
GaAs: Gallium Arsenide
HBT: Heterojunction Bipolar Transistor
ILD: Interlayer Dielectric
LEDs: Light Emitting Diodes
PHEMT: Pseudomorphic High Electron Mobility Transistor
VASE: Variable-Angle Spectroscopic Ellipsometer