

Low-Cost, High-Performance Multifunction X-band Control MMICs Using Ion-Implanted FET Technology

Monte Drinkwine, Hausila Singh and Mike Ashman

M/A-COM, Inc., 5310 Valley Park Drive, Roanoke, VA 24019
Phone: 540 563-8600, E-mail: drinkwim@tycoelectronics.com

Abstract

To address increased performance requirements for X-band control circuits, a new switch FET, with a typical R_{on} of $1.6 \Omega \cdot mm$ for lower insertion loss, and a new gain FET, with high-drive capability and improved linearity, were developed and added to the suite of MSAG™ devices. These new MSAG FETs are fully compatible with other FETs in the MSAG suite. In this respect, MSAG stands alone with its demonstrated ability to combine the disparate functions required to produce a single-IC T/R control circuit, such as the one described herein, without sacrificing performance or reliability, and at affordable cost.

INTRODUCTION

The MSAG process is an ion-implant, refractory-gate, planar, self-aligned MESFET process used for making a wide range of MMICs operating from below 1GHz up to 20GHz. The first FETs in the MSAG process family were developed in 1987 as an extension of a SAG process technology originally intended for fabricating LSI digital circuits [1,2]. The ability to extend this basic SAG technology to MMIC applications relied on a planarization technique for adding a high-conductivity metal overlay to the gate electrode and a method for tailoring the conductivity of the channel, particularly in and beyond the drain-side access region. The baseline process approach used for making FETs in the MSAG process is shown in Figure 1. An SEM picture of a typical MSAG microwave FET is shown in Figure 2 where the gold metal gate overlay and asymmetric drain region are clearly depicted. This process approach has tremendous FET-design versatility as can be seen by illustrations of MSAG FET cross sections in Figure 3 where channel source-gate spacings, gate dimensions, gate overlay dimensions, channel conductivity and thickness, drain-side conductivity, and lateral conductivity profile have been changed to tailor devices for specific performance requirements and applications.

In concert with the ability to design or tailor a FET for a specific application (e.g., digital, switch, low-noise, power), this processing approach allows one to fabricate any of the devices shown in Figure 3 on the same integrated circuit. Thus, the idea behind the term “multi-function” is not limited to just making many different types of FETs, but it provides flexibility to design, in concert with each and every FET type available under the MSAG umbrella, to achieve a complex set of performance requirements *within one IC*.

The multi-function single-chip design approach, made possible with MSAG technology, is particularly advantageous in module design applications, such as phased array radar systems, where high complexity and high performance

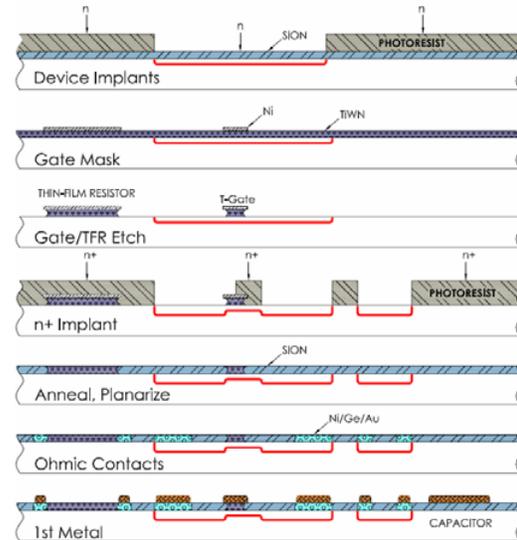


Figure 1. MSAG FET fabrication process flow.

are required *at affordable cost*. In such applications, modest cost savings at the module level result in significant savings at the array level. In a multi-chip module, when factors such as off-chip components and assembly costs are taken into account, MMIC-related costs can be significantly more than just the cost of the MMIC die. Thus, multi-function MMICs reduce cost through reduced MMIC die count and associated off-chip components and bond wires, while at the same time providing indirect savings through improved module yield and reliability.

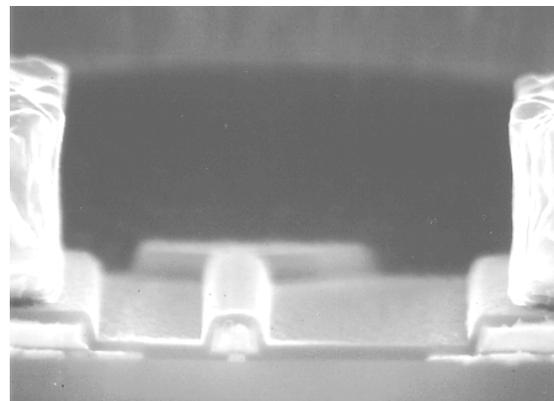


Figure 2. SEM cross section photo of a typical MSAG microwave FET.

Prior to the effort described in this paper, the MSAG suite of high-performance FETs, shown in cross section in Figure 3, consisted of:

5A: An asymmetric FET with high conductivity channel and high gate-drain breakdown voltage. Used primarily for high power applications, but also for low and medium power signal amplification.

5N: A symmetric FET with thin channel, low capacitance, and high conductivity access region. Used for low-noise applications.

5B: A symmetric FET with deep channel, and medium conductivity. Used for robust switching applications.

5E (5D): A symmetric FET-pair with thin channel, high conductivity access region, and positive threshold (negative threshold). Used in DCFL digital circuit applications.

This suite of FETs has been used very successfully in the design and fabrication of complex, high performance control circuits used in phased-array radar and communication systems up through X-band [3]. However, advanced system requirements for reduced losses and improved linearity (for enhanced detection and tracking in cluttered and/or jamming environments), dictated improvements in both design and device performance.

As a result of M/A-COM's latest efforts to satisfy advanced system performance requirements, two new MSAG FETs were developed. A switch FET with a typical R_{on} of $1.6 \Omega \cdot \text{mm}$ was developed to address the need for lower insertion loss; and a high-drive, high-linearity gain FET was developed to address the requirements for higher TOI. Both of these new MSAG FETs are fully compatible with other FETs in the MSAG suite, making it possible to design and fabricate low-cost, high-performance control circuits of high complexity such as the T/R control MMIC described herein.

FET DEVELOPMENT

A constraint was placed on the FET development: in order to be compatible with the existing MSAG suite of FETs, no new technology would be allowed. Therefore, this effort

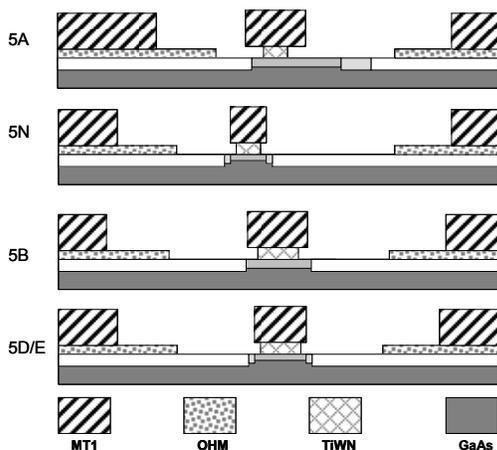


Figure 3. Cross section drawings showing layout and implant differences for the family of high performance MSAG FETs.

concentrated on adjusting device dimensions and channel conduction characteristics, both lateral and vertical. In order to keep the number of experiments and variants investigated at a reasonable and practical level, Design-of-Experiment methodology was used to investigate the large set of dimensional factors and levels in an efficient manner.

Switch FET: Development effort for the switch FET focused on reducing all sources of resistance, with constraints placed on keeping off-capacitance low and breakdown voltage as high as possible, consistent with a maximum gate control voltage of about -5V (available with MSAG digital control logic). The baseline switch (B) FET, shown in Figure 3, exceeded minimum spacing rules for the standard process, so it was possible to reduce resistance by reducing dimensions, particularly the ohmic-ohmic spacing, without need for a technology enhancement. As a switch FET, it was important to maintain symmetry on both sides of the gate, so maximum benefit was derived from the self-aligned feature of the MSAG process for keeping resistance low. Implant parameters were optimized for the channel region directly under the gate to further reduce resistance (and increase I_{dss}) while keeping full-pinch-off voltage within range of the digital logic control voltage.

Gate resistance is not as important for a switch FET as it is for an amplifier FET, so devices with and without a metal gate overlay were fabricated for comparison. Results showed that for a switch FET of modest finger length, the gold metal overlay on the gate was not necessary to maintain performance up through 20GHz and that without the metal overlay, capacitance was reduced, thus producing an improvement in overall performance when used in a switch circuit.

DC and RF FET characterization was used to guide much of the development effort. But, as a real test for the impact on performance, a standard evaluation single-pole-double-pole (SPDT) switch was used to characterize and validate FET modifications for improvement via measurements of insertion loss and isolation from 2 to 20 GHz. This simple circuit, shown in Figure 4, proved invaluable in determining the optimum level for some of the more subtle-effect factors. The final-version switch FET, termed the C FET is shown in cross section in Figure 5; its characteristics are shown in comparison to the baseline switch (B) FET in Table 1.

Gain FET: One of the most demanding and most difficult-to-achieve performance parameters for control circuits is linearity or TOI, which is required for the reasons cited previously. Design efforts aimed at improving TOI using the MSAG process were successful up to a point but analysis showed that the type A gain FET used in the final gain stages was limiting TOI performance.

Two additional characteristics were also targeted for improvement: recovery time and output phase stability. In a radar application, the gain FETs must be robust against overdrive conditions that can be created by jamming. If any changes occur during overdrive, the FETs must recover to their original characteristic behavior quickly. Therefore, our

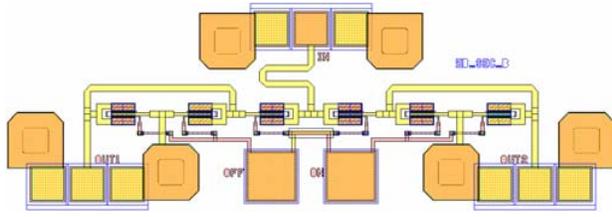


Figure 4. Layout showing the Single-Pole-Double-Throw switch circuit used to help characterize the effect of FET variants.

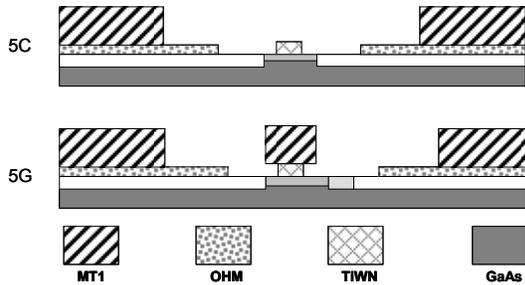


Figure 5. Cross section drawings showing layout and implant configurations for the improved switch (C) and gain (G) FETs.

	FET Type				Units
	B vs C	A vs G	A vs G	A vs G	
I_{dss}	255	360	390	400	mA/mm
V_t	-2.65	-2.45	-2.75	-2.80	V
BV	12.5	10.5	19	13	V
R_{on}	2.2	1.6			$\Omega \cdot mm$
C_{off}		380			fF/mm
G_m			115	140	mS/mm
C_{gs}	830		1300	960	fF/mm

Table 1. Comparison of key PCM parameters for baseline (B and A) and new (C and G) switch and gain FETs..

gain FET development effort focused on creating a new MSAG FET with improved linearity and high P1dB for 5V operation, and robustness with respect to recovery time after exposure to over-drive conditions.

A comparative evaluation of existing MSAG FETs showed that the A FET, with its already-high P1dB characteristic, should be a good starting point to work from. The A FET was designed and optimized for high saturated-power amplifier applications, and within the context of the MSAG process, an asymmetric channel structure with a lightly-doped drain region had been found to work best for providing the high breakdown voltage needed to operate at 10V and produce the power density required. Conversely, there were indications that the highly asymmetric design of the AFET was, in part, responsible for limiting TOI below the desired value and hindering recovery time. Thus, our gain FET development effort focused on optimizing the conduction and doping profile characteristics in the channel on the drain side

of the FET. The multiple-selective implant feature of the MSAG process lends itself well to such an optimization, with a continuum of spacings, lateral doping profiles, and vertical doping profiles that can be implemented.

As with the switch FET development, Design-of-Experiment methodology was used to efficiently reduce the scope of investigation. However, unlike the switch FET development effort, there were no easy-to-measure FET figure-of-merit parameters that had direct connection to the important performance parameter TOI, so most of the decision making for optimization of the FET came from measurements of an SEC (like that shown in Figure 6), with DC and RF FET measurements providing constraint limitations such as breakdown voltage, V_t , C_{gs} , etc.

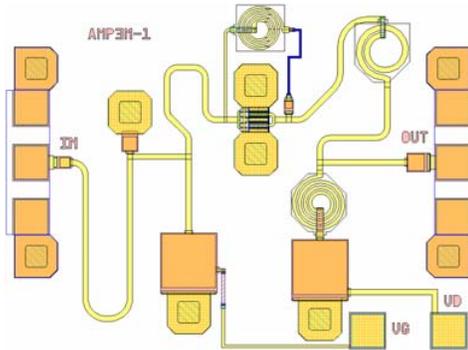


Figure 6. Layout showing the Amplifier circuit standard evaluation circuit (SEC) used to help characterize the effect of FET variants for the gain FET development.

As an example of this approach, Figure 7 shows the combined results of TOI+P1dB vs implant spacing on the drain side of the gate. Also note in Figure 8 a similar correlation plot for breakdown voltage (BV) and dc Ipeak vs implant spacing on the drain side of the gate. Consequently, the drop in BV with a decrease in drain-implant spacing places an upper limit on TOI improvement with the constraint of a particular operating voltage. The final-version gain FET, the G FET, optimized for TOI and 5V operation, is shown in cross section in Figure 5 and its characteristics are shown in comparison to the baseline gain (A) FET in Table 1.

Because both of these new FETs (C and G) are essentially variants on existing MSAG FETs, all the same characteristics of excellent uniformity across-wafer and high yield are inherent in their behavior. In addition, initial studies show these new devices exhibit excellent reliability characteristics like other MSAG devices.

CIRCUIT PERFORMANCE RESULTS

Using the evaluation circuit depicted in Figure 4, same-wafer performance evaluations were made comparing the new (C) and baseline (B) switch, as shown in Figure 9. A 25% reduction in insertion loss and improvement in isolation over the frequency range 6-18 GHz were obtained using the new switch FET. Linearity results from a breakout circuit comparing the baseline (A) and new (G) gain-FET are shown in Figure 10. The X-band MCM receive output TOI of this

circuit is, on average, 4 dB higher when the new gain FET is used. Transmit P1dB and recovery time were also shown to be improved with the new gain FET. Using the new MSAG switch and gain FETs, along with power and digital FETs, the complex single-chip control circuit shown in Figure 11 was designed and fabricated. Circuit design and performance details for this IC are found elsewhere [4].

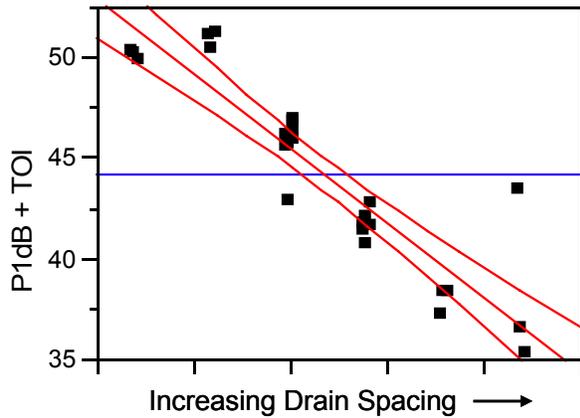


Figure 7. Effect of drain-implant spacing on TOI+P1dB.

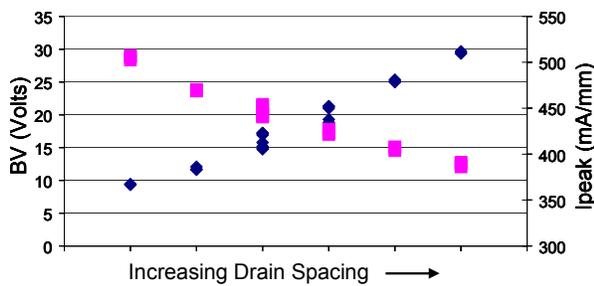


Figure 8. Correlation between BV, Ipeak, and drain-implant spacing.

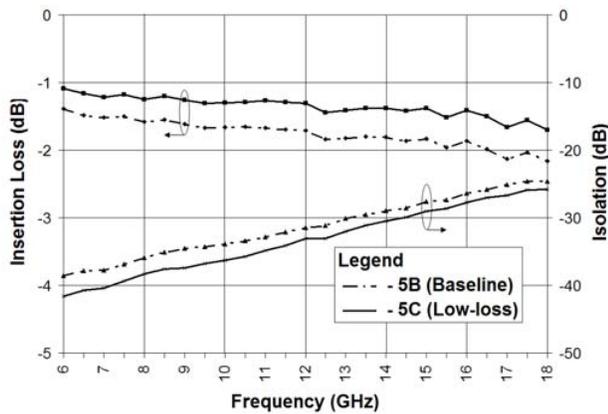


Figure 9. Switch evaluation circuit comparing insertion loss and isolation with the new switch (C) FET versus the baseline switch (B) FET.

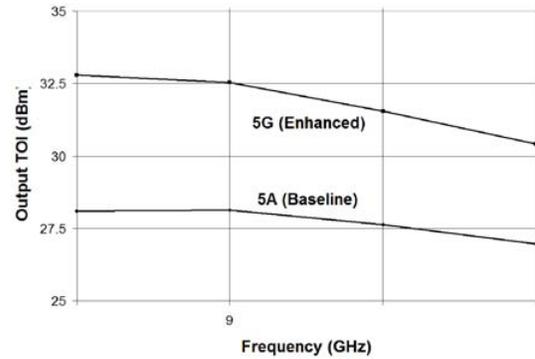


Figure 10. X-band MCM receive output TOI comparing new (G) gain FET with baseline (A) FET.

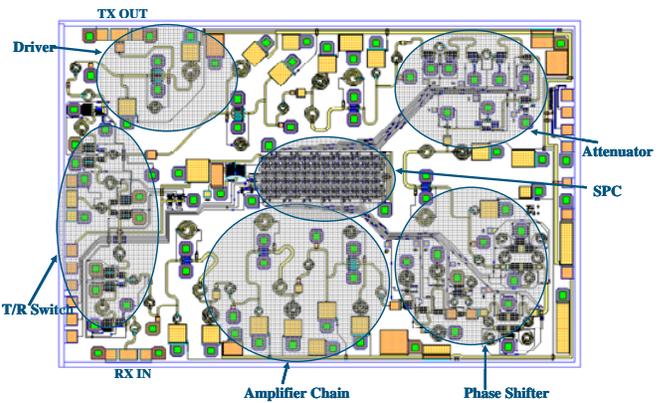


Figure 11. Layout of a control IC designed using A, C, D/E, G, and N FETs. It has seven stages of gain, six-bits each of phase and attenuation control, transmit/receive switching and an onboard serial-to-parallel controller.

CONCLUSION

A new MSAG switch FET with a typical R_{on} of $1.6 \Omega \cdot \text{mm}$ was developed to address the need for lower passive circuit insertion loss. A new MSAG FET with high-drive and high-linearity was developed to address requirements for higher TOI. Using the improved switch FET, insertion loss has been decreased by $\sim 25\%$ in switch applications. Using the new gain FET, MCM receive output TOI has been increased by more than 4 dB for the X-band MCM data presented. Both of these new MSAG FETs are fully compatible with other FETs in the MSAG suite making it possible to design and fabricate higher-performance, low-cost multi-function control circuits.

ACKNOWLEDGEMENTS

Many thanks to Mark Flora for special FET testing and implementation of the PCM measurement for C_{off} . Thanks to Inder Bahl for help in physical modeling of the switch FET.

REFERENCES

- [1] R. A. Sadler, A. E. Geissberger, H. P. Singh, and M. L. Balzan, *10th European Specialist Workshop on Compound Semiconductor Integrated Circuits*, Visby, Sweden (1986)
- [2] A. E. Geissberger, R. A. Sadler, E. L. Griffin, I. J. Bahl, and M. L. Balzan, *IEEE Trans. Electron. Devices*, vol. 35, pp. 615-622 (1988)
- [3] H. Singh, *Microwave Product Digest*, (August 2003)
- [4] H. Singh, M. Ashman, and M. Drinkwine, *RF Design*, October 2006, pp. 8-11.