Gate Shorts: A Process Engineer's Nightmare

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Abstract

Gate shorts are devastating for the basic function of a FET. For one of TriQuint Semiconductor's SAG-pHEMT processes two sources of gate shorts were found and eliminated. The dominant source of gate shorts was the accumulation of ohmic metal on a ledge of unexposed photo resist. That could be fixed by varying the Focus Offset on the stepper during exposure of the ohmic photo layer. The secondary source was residue underneath ohmic metal. This residue could be removed by a wet clean.

INTRODUCTION

For one of its SAG pHEMT processes [1], TriQuint Semiconductor uses an evaporated AuGeNi metal stack [2] to form the ohmic contacts and the thick gate reinforcement in one process step as shown in Figure 1.

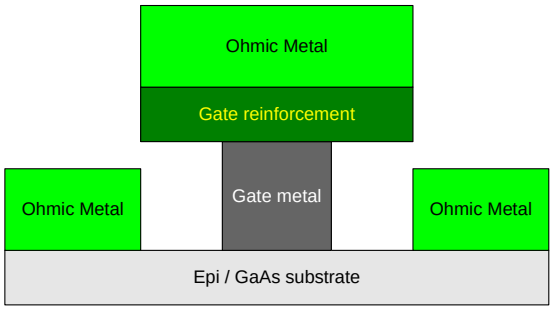


FIGURE 1: Schematic cross section of a FET

During high volume production we faced a high yield loss at die sort due to shorted gates. This paper reviews the two main sources of this issue, the electrical screening, and how the issues were solved.

DESCRIPTION OF THE GATE SHORTS

Failure Analysis of die sort fails revealed two kinds of gate shorts on this process. Figure 2 shows a typical example of a filament between gate and the corner of ohmic metal forming the drain or source of the FET. This filament was the main cause of yield loss. Given its small size, the filament can be burned away during parametric testing, which makes it difficult to detect. Also, it is literally invisible at microscope visual inspection.

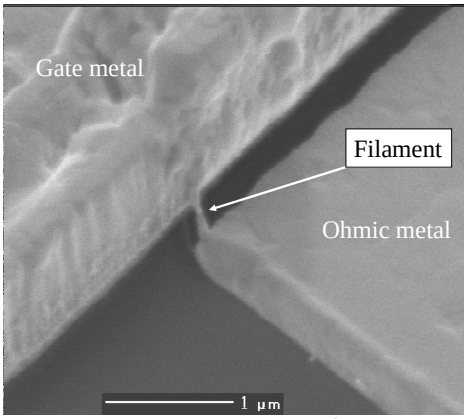


FIGURE 2: Fine short at the corner of ohmic metal

A smaller yield loss was caused by gate shorts as shown in Figure 3. These can be found along any part of the gate and are much more robust. They are fairly easy to detect at parametric test and are visible at microscope visual inspection.

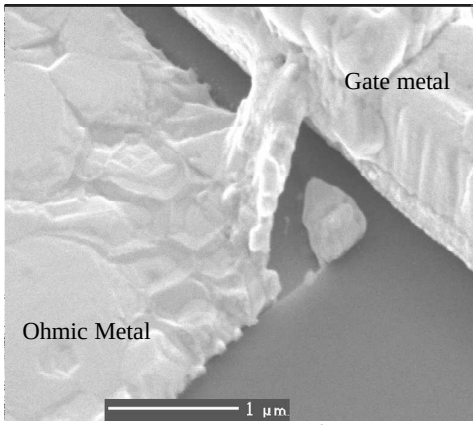


FIGURE 3: Coarse short which can be found along the gate

ELECTRICAL SCREENING

Screening for gate shorts is done during wafer fabrication on the process control monitors (PCM) and at the product level at die sort.

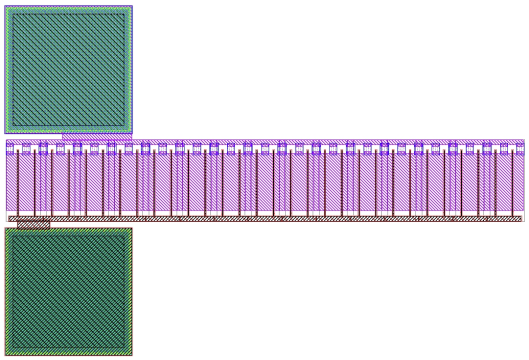


FIGURE 4: PCM test structure to detect gate shorts

The PCM test structures include a Gate-Ohmic leakage comb which is shown in Figure 4. It contains 30 gates above non-active area with a total perimeter of 2700 µm. The test of this structure is a simple applied voltage with a measurement of the resulting current. The voltage level has to be picked carefully since the fine filaments can be burnt away if the current density gets too high. Typical values for a short-free comb are 1 pA/µm at 1V bias and 6 pA/µm at 3V bias. If shorts are present, current levels are above 5 µA/µm and even hit the compliance of the test which is set to 1 µA/µm at 1V bias and 100 µA/µm at 3V bias.

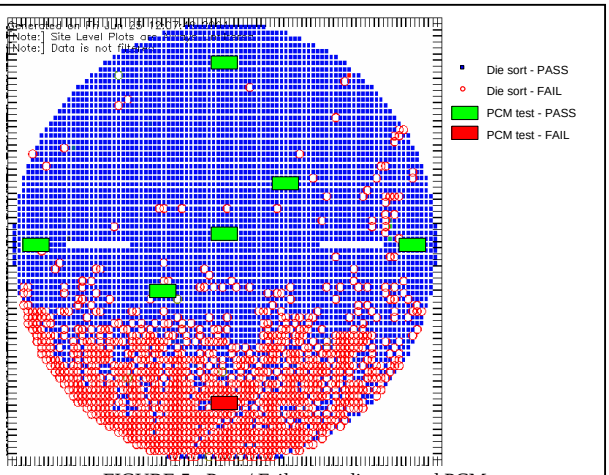


FIGURE 5: Pass / Fail map - die sort and PCM

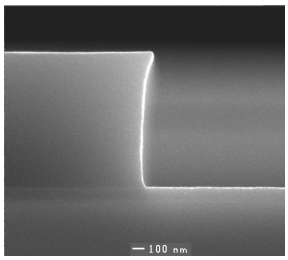
Although a sensitive PCM test is available to detect gate shorts, an effective screen can be cumbersome. The density of PCM structures on the wafer is limited. This can lead to the case where just one PCM failed test, but a significant number of FET's on product die suffers shorted gates. To overcome this issue a screen at die level has been developed. This test is executed on a direct accessible FET of the product die. The gate is biased in reverse direction with a voltage low enough not to burn away the filaments and too low to turn on the Schottky diode.

Figure 5 shows a Pass / Fail map of a wafer, with die sort and PCM test overlaid. As one can see, a single PCM test fail can translate into a high number of lost die on a wafer.

The implemented die sort test provided the best screen available for this issue and was used to demonstrate both process and yield improvement.

PROCESS STABILIZATION - LITHOGRAPHY

The pass/fail maps of the die sort test were crucial for the solution of the dominant source of gate shorts. Those maps showed a print field dependent pattern which pointed to a lithography related problem. Several experiments were executed covering exposure and photo resist develop parameters as well as metal deposition conditions.



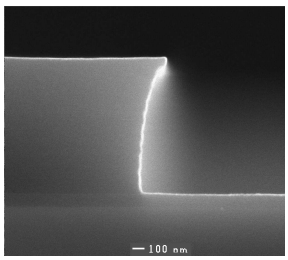


FIGURE 6: Resist profile with different FO: left image positive FO, right image negative FO

The data analysis of all experiments showed that the Focus offset (FO) on the steppers strongly impacts the formation of the fine filaments between the gate and the ohmic metal corners shown in Figure 2. Table 1 gives an overview of an FO experiment that indicated the needed change for improving the process.

TABLE I
FOCUS OFFSET (FO) EXPERIMENT

Dose	FO	Develop time	Failure rate DS
Standard	Standard	Standard	6.2%
Standard	Negative	Standard	1.7%
Standard	Positive	Standard	88.8%

The focus offset has an impact on the resist profile as shown in Figure 6. The negative FO produced a more re-entrant profile with a protruding ledge. This proved effective at eliminating growth of evaporated metal at the corner of the ohmic features.

To explain the function of the more re-entrant profile, one has too look at how the resist covers the gate just before ohmic metal deposition as shown in Figure 7. Underneath the gate reinforcement, a ledge of unexposed resist can be

found which can not be cleared during the photo resist development. At ohmic metal deposition, metal can accumulate on that ledge and create a short. A more reentrant profile acts as an umbrella, preventing metal accumulation on the photo resist ledge.

The implementation of a negative FO at the steppers for the ohmic metal layer eliminated the yield loss due to fine filaments between the gate and the corner of ohmic metal.

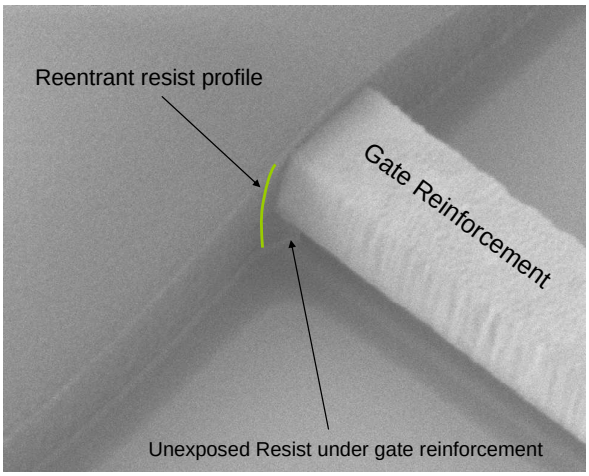


FIGURE 7: Resist covering gate before ohmic metal deposition

PROCESS STABILIZATION - CLEANING

The gate short pictured in Figure 3 can be characterized as a randomly distributed defect, which was responsible for the smaller part of die sort fall out. It is not limited to the area close to the gate and can be found in any ohmic feature. Figure 8 shows an example of this defect within a larger feature. Due to its shape this defect has been named 'Ohmic Volcano'.

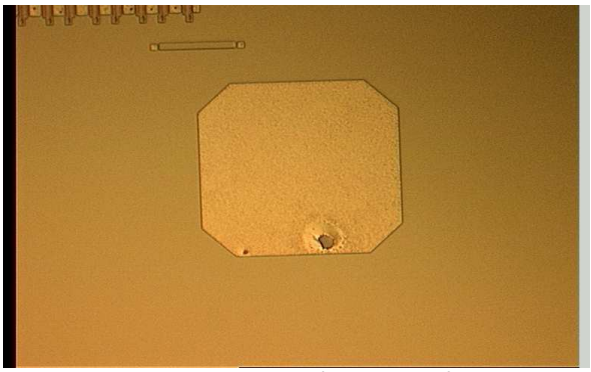


FIGURE 8: Ohmic metal defect on a larger feature

The defect is not visible until the alloy of the ohmic contacts. Our investigations showed that this defect occurs when residue is left behind by the passivation etch just before the ohmic metal deposition. At high temperatures during alloy, the residue vaporizes and blows parts of the ohmic metal away, which can create the shorts if gates are near.

During our investigations we found that the solubility of the residue is largely dependent on the pH of the pre-cleaning solution. We found that a wet clean with a different pH value completely removes the residue and therefore this type of defect.

CONCLUSION

Gate shorts are devastating for the basic function of a FET. We found two contributors to gate shorts on one of TriQuint Semiconductor's SAG-pHEMT processes.

The major type of gate shorts was identified as fine filaments at the corners of ohmic metal features. This was fixed by varying the stepper parameter Focus Offset during the exposure of the ohmic photo layer. A negative FO creates an umbrella effect preventing the accumulation of metal on a photo resist ledge.

The minor type of gate shorts was characterized as an ohmic metal defect. The defect occurs when residue is left on the substrate surface after the etch of the passivation. This residue evaporates at alloy and blows ohmic metal away, which can cause a short if this happens close to a gate. A wet clean with a different pH value increases the solubility of this residue and it prevents the formation of the ohmic metal defect.

ACKNOWLEGDEMENTS

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REFERENCE

[1] Gerard Mahoney et al, "Transfer of GaAs pHEMT Technologies from Infineon to TriQuint", CS MANTECH, May 2004
[2] Thorsten Saeger et al, "Visual and Electric Ohmic Metal Degradation From Later Process Steps", CS MANTECH, April 2005

ACRONYMS

FO	Focus Offset
FET	Field Effect Transistor
SAG	Self Aligned Gate
PCM	Process Control Monitor