Hydrogen Incorporation of Metal Gate HfO_2 MOS Structures on $In_{0.2}Ga_{0.8}As$ Substrate with Si Interface Passivation Layer

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ABSTRACT

Recently, we have investigated the GaAs MOSFET and InGaAs MOS structure using Si interface passivation layer (IPL) and HfO_2 as gate dielectric. In this work, we have investigated hydrogen incorporation effects for $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL and H_2 annealing at 500°C for 30min. Excellent electrical characteristics with Low Dit (~$2.8 \cdot 10^{12}$) with low frequency dispersion (< 0.1% and <10mV) has been obtained.

I. INTRODUCTION

High-k dielectrics, such as HfO_2, have been considered as alternative to SiO_2 in Si-based CMOS technology. The alternative dielectrics provide excellent opportunity for considering alternative substrate materials such as SiGe [1-2]. The advantages of high electron mobility of InGaAs have long been recognized, and many efforts to fabricate MOS transistors have been pursued. The key challenge for III-V-based MOSFETs is the lack of high-quality, thermodynamically stable insulators that passivate the interface states and prevents Fermi level pinning at III-V-gate dielectric interface [3]. We have recently demonstrated effective passivation of GaAs [4-6] and investigated the InGaAs MOSCAP using Si IPL and HfO_2 as gate dielectric. Electrical characteristics with thin EOT (~2.5nm), low frequency dispersion (<5%) were reported. The thickness of the Si IPL and PDA time were correlated with C-V characteristics [7]. Extensive experimental and theoretical investigations have been undertaken to understand the incorporation behavior of hydrogen into semiconductors, especially in Si and GaAs. In this work, we have studied hydrogen incorporation effects for $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL and H_2 annealing at 500°C for 30min. Excellent C-V characteristics with Low D_{it} (~$2.8 \cdot 10^{12}$) with low frequency dispersion (< 0.1% and <10mV) has been obtained.

II. EXPERIMENT

MOS capacitors were fabricated on MBE grown n-type InGaAs wafer doped with Si. A cross-sectional view of the MOSCAP is shown in Fig. 1. The surface oxides were removed with a HCl clean followed by $(NH_4)_2S$ dip, resulting in a clean S-passivated GaAs surface. Then Si IPL was deposited by sputtering of Si in Ar ambient at 400°C. PVD HfO_2 films were deposited using the modulation technique [8], followed by PDA at 600°C in N_2 (O_2 5%) ambient. The thickness of Si IPL layer varied from ~9Å (90sec deposition time) to ~12Å (2min); and the physical thickness of HfO_2 layer was ~ 100Å. PDA TaN was used as gate electrode. After gate patterning using reactive ion etching (RIE) based on CF_4 gas, low-resistance ohmic contact was formed by using AuGe/Ni/Au alloy on the backside of the wafer [9]. The samples were then annealed at 450°C for 30sec in nitrogen. Electrical characterization was performed on MOS capacitors before and after H_2 annealing at 500°C for 30min. EOT values were extracted using a C-V simulation program. [10].

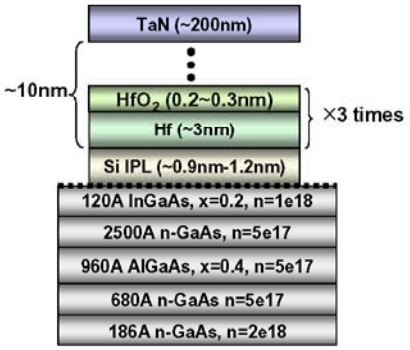

Figure 1. A cross-sectional view of the n-InGaAs MOSCAP structure

III. RESULTS AND DISCUSSION

X-ray photoelectron spectroscopy (XPS) showed that with 500°C and 600°C 1min PDA, Si was partially oxidized, and after 600°C 3min PDA, the Si IPL was oxidized to SiO_2 (Fig. 2a). While the As-O bonds were observed after anneal, no other distinguishable bonds were observed. As shown in Fig. 2b, As_2O_3 was obtained due to PDA anneal.

PDA above 600°C resulted in a much higher As_2O_3 intensity than the 500°C PDA.

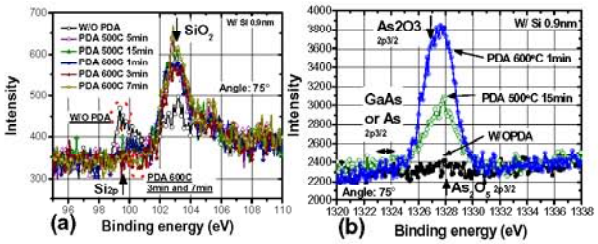

Figure 2. (a) XPS spectra of the Si 2p (b) As 2p for 90sec (~0.9nm) Si IPL with different PDA time

Typical C-V characteristics of TaN/HfO2/Si/$In_{0.2}Ga_{0.8}As$ as function of frequency after H_2 annealing for 1.2nm Si IPL are shown in Fig 3.

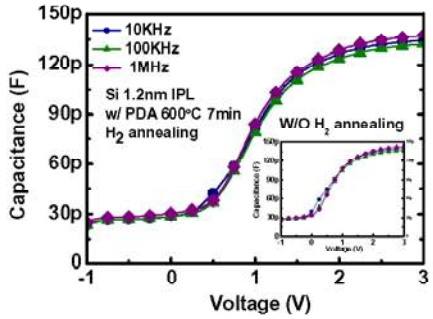

Figure 3. Frequency dispersion for 120sec (~1.2nm) Si IPL with PDA 600°C 7min

With increasing PDA temperature and time, flat band voltage shift negative direction however, after H_2 annealing, flat band voltage for all PDA samples shift positive direction with H_2 incorporation (Fig.4).

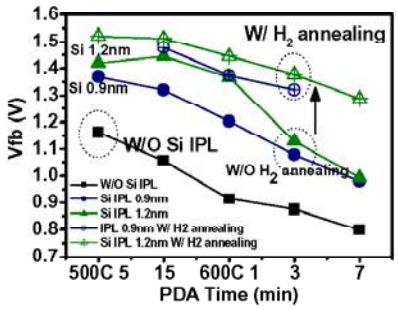

Figure 4. Flat band voltage shift as a function of PDA time

The slopes of the flat band voltage shift for with Si IPL and without Si IPL structure are similar to each other. The results suggest that flat band voltage shift was more affected by interfacial InGaAs oxide than Si oxidation and one of the clear contributions was As oxide (Fig. 2b) and hydrogen incorporation compensated the As oxide contributions. Fig. 5 summarize the frequency dispersion characteristics (% and ΔmV are defined in Fig. 5a) versus PDA time with different Si IPL deposition condition and hydrogen incorporation. In general, hydrogen incorporation resulted in slightly lower frequency dispersion (% and ΔmV). In contrast, without Si IPL, frequency dispersion was around 15~40%.

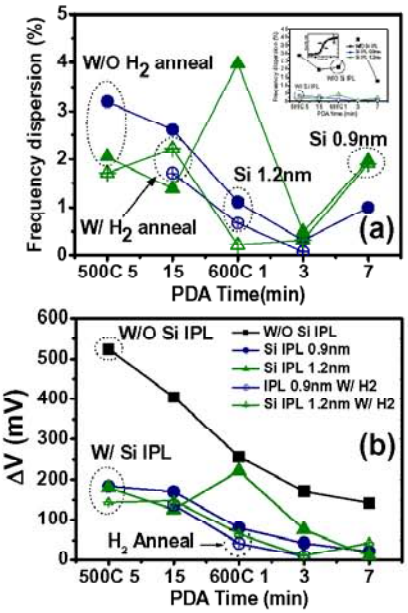

Figure 5. (a) Frequency dispersion (%) (b) ΔmV as a function of PDA time with different Si IPL thickness

Hydrogen incorporation resulted in similar hysteresis (mV) and EOT values (Fig.6 and Fig. 7).

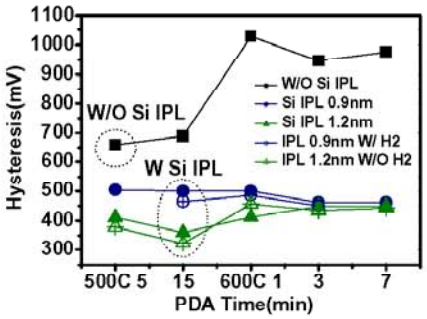

Figure 6. Hysteresis as a function of PDA time with different Si IPL thickness

Thin amorphous Si IPL between HfO_2 and InGaAs substrate with hydrogen incorporation did not significantly contribute to hysteresis characteristics which are more significantly affected by bulk HfO_2 than interface and to EOT change. Even though EOT is thinner for sample w/o Si IPL layer, the

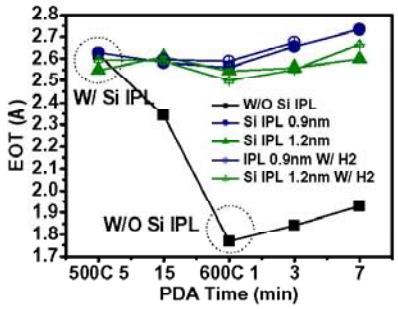

Figure 7. EOT as a function of PDA time with different Si IPL thickness

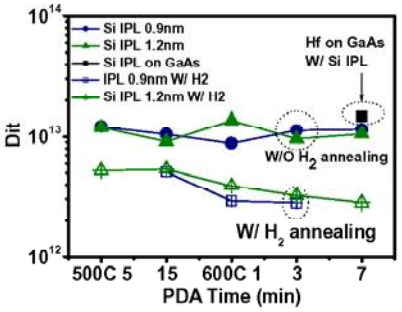

Figure 8. D_{it} as a function of PDA time with different Si IPL thickness with H_2 annealing

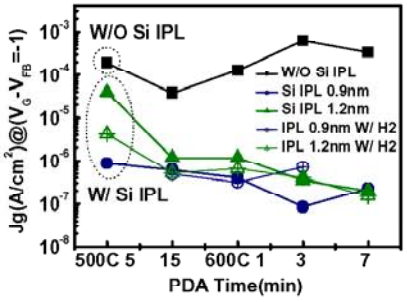

Figure 9. Leakage current as a function of PDA time with different Si IPL thickness

MOSCAPs exhibit high leakage, hysteresis and frequency dispersion. Si deposition time of 90 second (~0.9 nm) with 7min PDA time resulted in ~10^{13} D_{it} value which was similar to GaAs based structure using conductance method (Fig. 8). Hydrogen incorporation samples resulted in lower Dit value ~2.8×10^{12} (~4 times less than W/O H_2 annealing). Si IPL with hydrogen incorporation led to similar leakage current (Fig. 9 and Fig. 10) which was less than the same structure with GaAs substrate.

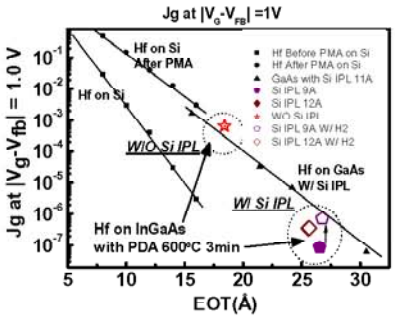

Figure 10. Jg versus EOT for H_2 annealing samples

IV. Conclusion

The electrical characteristics of TaN/HfO2/$In_{0.2}Ga_{0.8}As$ MOSCAP with H_2 annealing are reported. We studied the effects of H2 annealing with PDA time and Si IPL for the MOS capacitor with high-k (HfO_2) material on MBE grown $In_{0.2}Ga_{0.8}As$. Low D_{it} (~$2.8\cdot10^{12}$) with low frequency dispersion (< 0.1% and <10mV) has been obtained.

V. Acknowledgements

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ACRONYMS

EOT: Equivalent Oxide Thickness
IPL: Interface Passivation Layer
PDA: Post Deposition Annealing
RIE: Reactive Ion Etching
XPS: X-ray Photoelectron Spectroscopy