Advanced GaAs MMIC Fabrication Process with PIN Diodes for ESD Protection

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Abstract

Advanced GaAs MMICs with electrostatic-discharge (ESD) protection devices were developed. The ESD protection devices consist of anti-series connected PIN diodes, which are formed on a wafer with enhancement- and depletion-mode AlGaAs/InGaAs HJFETs. To realize high ESD tolerance, a constant capacitance at low bias, and low harmonics at high frequency, the PIN diodes were optimized in terms of Zenner-like characteristics. As for the GaAs MMICs with ESD protection devices, their survival voltages under a human-body model test are high (i.e., 2000 V). This promising ESD-protection device has been applied to MMIC products such as antenna switches and low-noise amplifiers. This technology has already been implemented in our mass-production processes for fabricating high-performance MMICs for "3-G" phones.

INTRODUCTION

Electrostatic-discharge (ESD) protection is a key technology of MMICs used in the front-end modules for high-frequency wireless systems such as cellular phones and W-LAN. In regards to the fabrication process for GaAs HJFET MMICs, E-mode HJFETs and Schottky-barrier diodes have already been developed as ESD protection devices [1-3]. However, such circuits using E-mode HJFETs are rather complicated, and the ESD protection ability of Schottky-barrier diodes is insufficient. To solve this problem, we have developed the new GaAs MMIC system with unique configuration. Its fabrication process directly combines enhancement- and depletion-mode (E/D-mode) AlGaAs/InGaAs HJFETs and PIN diodes.

In this paper, first, the device structure of our MMIC is reviewed. After that, its integration into the existing HJFET process flow is explained [4]. Next, the characteristics of the ESD-protection device are presented, and the structure optimization is explained. Finally, some applications of the MMIC are presented.

DEVICE STRUCTURE AND RPROCESS INTEGRATION

Our developed ESD-protection devices consist of anti-series connected PIN diodes, which are formed on a wafer with E/D-mode AlGaAs/InGaAs HJFETs, as shown in Fig. 1. The E/D-mode HJFETs are formed on a conventional double-doped and double-hetero-junction epi-structure [4]. The typical D-mode HJFET pinch-off voltage is –0.6 V with transconductance (G_m) of 350 mS/mm and breakdown voltage (BV_{gdo}) of –20 V. On the other hand, the typical E-mode HJFET pinch-off voltage is +0.3 V with G_m of 450 mS/mm and BV_{gdo} of –20 V. The epi-structure has four additional layers to that of existing HJFETs. That is to say, the n^+-InGaP, n^+-GaAs, i-GaAs, and p^+-GaAs layers are grown by metal-organic vapor-phase epitaxy (MOVPE). The p^+-GaAs layer is used for the ohmic contact of the anode, and the n^+-InGaP layer is used as the highly selective etch-stop layer.

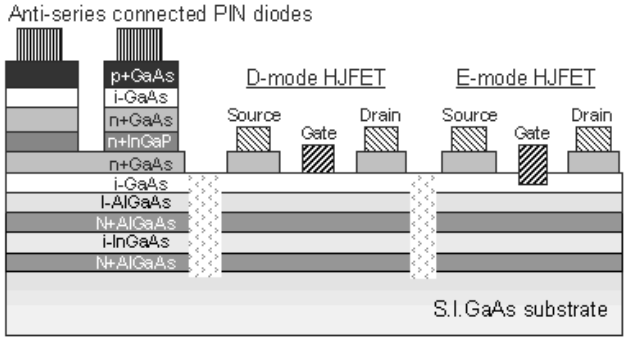

Figure 1: Schematic cross section of device structure

First, the GaAs layers (PIN structure) are etched above the InGaP etch-stop layer, and the InGaP layer is removed by another selective wet etching. After this procedure, the same processes used for the existing HJFETs are carried out [4]. For the ESD protection devices with the anti-connected PIN diodes, only anode electrodes are formed as shown in Fig. 1. The non-alloy ohmic-contact system of metal/p^+-GaAs makes it possible to form anode electrodes simultaneously with the other electrode or metallization. Only one additional mask and two additional etching steps are therefore added to the existing production HJFET process flow.

In the manner described above, PIN diodes and existing E/D-mode HJFETs are combined. The antenna switches (SW) and low-noise amplifiers (LNA) MMICs including these devices are realized using the same epi wafers. The pinch-off voltage of each MMIC is controlled by the recess

etch. To use the same epi wafers for several kinds of MMICs in this manner is very favorable for mass-production and contributes to cutting the cost of the epi wafers.

DEVICE CHARACTERISTICS AND OPTIMIZATION

The typical I-V and C-V characteristics of the developed ESD protection device, which consists of anti-series connected PIN diodes, are shown in Fig. 2. The protection device exhibits Zenner-like characteristics and has an almost constant capacitance in the low-bias region (from –7 V to 7 V). The breakdown voltage is set at about 8.5 V. These are important parameters for operating the circuit at high performance and to protect it against ESD damage.

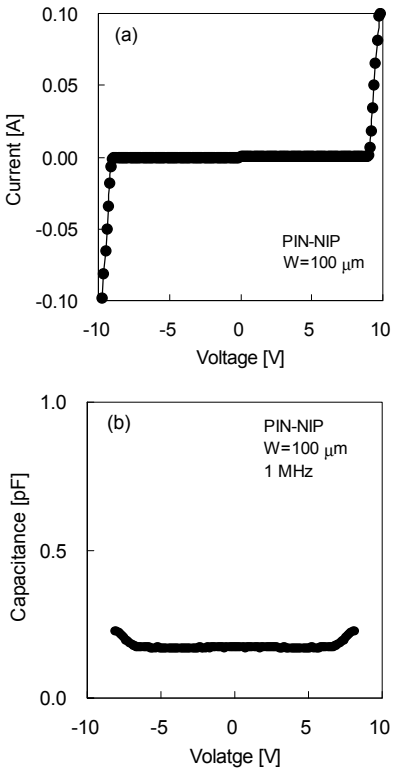

Figure 2: (a) I-V and (b) C-V characteristics of the ESD protection device

Figure 3 shows the harmonics characteristics of the ESD protection device as a function of input signal power. The level of the harmonics is not negligible for the MMICs. The appropriate size of the ESD protection device must thus be selected on designing the circuit.

The dependencies of i-GaAs thickness on several device parameters are shown in Fig. 4. The i-GaAs thickness fairly strongly influences breakdown voltage, junction capacitance, series resistance, and ESD tolerance. The thickness of the device is set to the optimum value of 70 to 200 nm under consideration of circuit performance. In the case of a high-power RF signal input, that is, high voltage swing, some ESD protection devices are connected in series (stack structure).

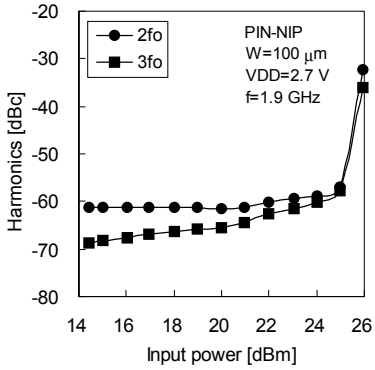

Figure 3: Harmonics characteristics of the ESD protection device

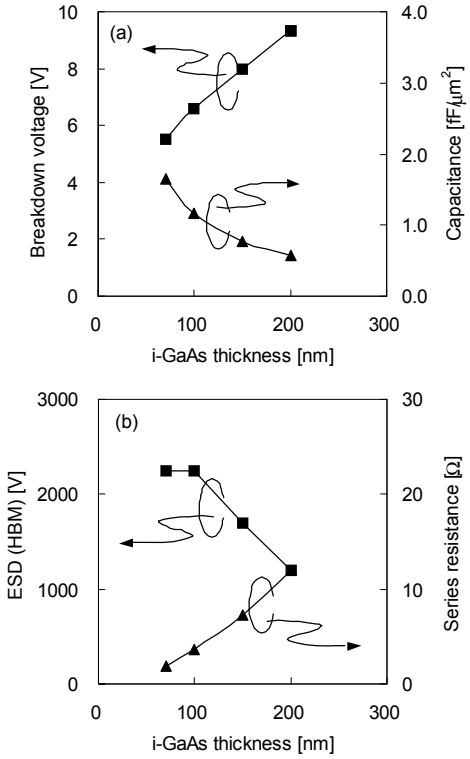

Figure 4: (a) Breakdown voltage and capacitance vs. i-GaAs thickness of the ESD protection device and (b) ESD(HBM) and series resistance vs. i-GaAs thickness of the ESD protection device

The size dependencies of the ESD protection device were investigated in detail in order to confirm ESD tolerance. The 3D scheme of the ESD protection device is shown in Fig. 5. Junction length (L) and unit junction width (Wu) are defined as shown in Fig. 5. Total junction width (W) is expressed as $W = Wu \times (n-1)$, where n is the total number of PIN junctions. Figure 6 shows ESD tolerance dependence on L and W. ESD(HBM) is the ESD survival voltage of a human-body model test, and ESD(MM) is that of a machine-model test. As shown in Fig. 6(a), ESD(HBM) and ESD(MM) are

saturated with increasing L. The use of large L is not appropriate for shrinking the area of the ESD protection device. On the other hand, ESD(HBM) and ESD(MM) have a linear dependence on W. It is therefore possible to design the ESD tolerance by selecting the appropriate W of the ESD protection device.

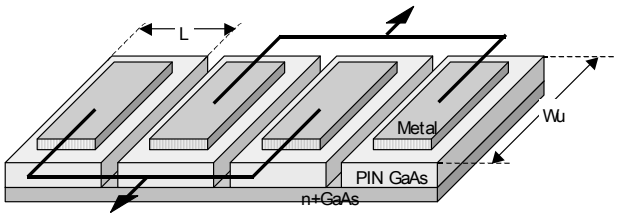

Figure 5: 3D schematic view of the ESD protection device

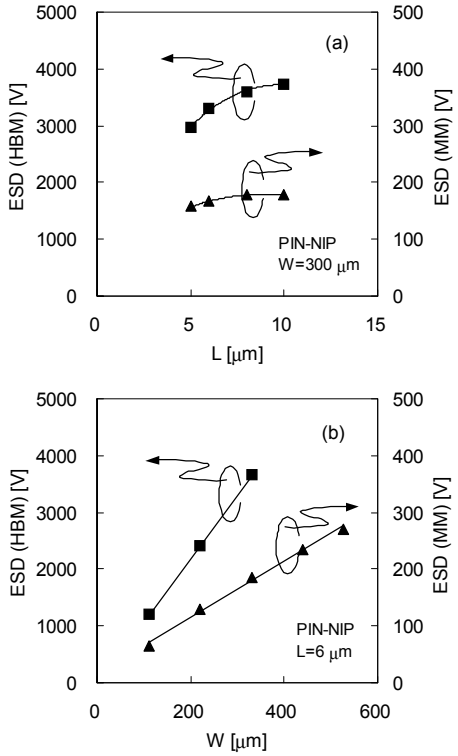

Figure 6: (a) ESD(HBM) and ESD(MM) vs. L;
(b) ESD(HBM) and ESD(MM) vs. W

The second-harmonics dependence on impedance (Z) of the ESD protection device is shown in Fig. 7. Several kinds of ESD protection devices with different W and number of stacks were measured at high frequency (1.9 GHz). The harmonics levels have a linear relationship to $1/Z^2$. This result is probably attributed to the change of junction capacitance caused by the DC bias and RF signal input.

As mentioned above, it is possible to design the ESD tolerance and the harmonics of the ESD protection devices. It is therefore important to attain a higher ESD tolerance while keeping lower harmonics and by using a smaller device.

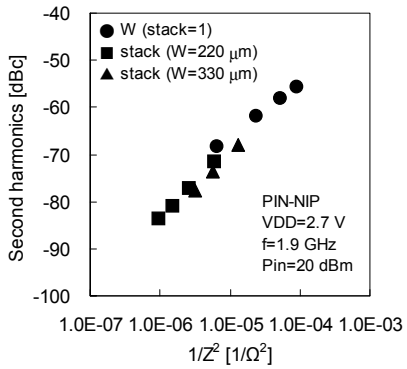

Figure 7: 2nd harmonics vs. $1/Z^2$

DEMONSTRATION OF APPLICATIONS

The effective ESD-protection technology that we developed was applied to MMIC products such as SW and LNA. Figure 8 shows a photograph of GSM/W-CDMA DP7T SW implemented with a 4-bit-control-logic circuit. Table 1 summarizes the DP7T SW performance. While high ESD tolerance of 200 V or more ESD(MM) and 3000 V or more ESD(HBM) on all pins is maintained, high SW performance (namely, low loss, high linearity, and low harmonics) is realized. A SW implemented on a chip with this logic circuit is superior in terms of product size to another company's SW constructed with the GaAs SW IC and the Si CMOS logic IC [5].

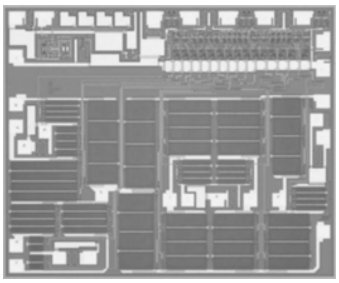

Figure 8: Photograph of GSM/W-CDMA DP7T SW

Figure 9 shows a photograph of the ESD protection device used in an LNA IC for digital television (DTV). The ESD protection devices are connected at all pads. Figure 10 shows the gain and NF characteristics of the DTV LNA, and Table 2 summarizes its performance. With keeping high ESD tolerance of 130 V or more ESD(MM) and 2000 V or more ESD(HBM) on all pins, high LNA performance, namely, high IIP3, high P-1dB, and low drive current, is realized.

TABLE 1: Performance of DP7T SW

Loss	0.35 dB typ.@WCDMA800 TRX 0.45 dB typ.@WCDMA1700/1500 TRX 0.45 dB typ.@WCDMA2000 TRX 0.60dB typ.@GSM850/900 TX 0.80dB typ.@ GSM850/900 RX 0.85dB typ.@GSM1800/1900 TX 1.10dB typ.@GSM1800/1900 RX
Harmonics	2fo=-44 dBm typ.@GSM850/900TX , +34.5 dBm 3fo=-40 dBm typ.@GSM850/900TX , +34.5 dBm 2fo=-47 dBm typ.@GSM1800/1900TX , +33 dBm 3fo=-45 dBm typ.@GSM1800/1900TX , +33 dBm IMD2=-112 dBm@840 MHz,+20 dBm IMD3=-109 dBm@1950 MHz,+20 dBm
VDD range	2.6-3.0 V
Current drain	600 uA@26 dBm
Vcontrol (L)	0.45 V
Vcontrol (H)	1.3 V

The fabrication process has already been implemented into our mass production processes and been used to produce high-performance MMICs for "3-G" mobile phones. Through the development of these ESD protection devices, higher integration in MMICs has also become possible as a result of the reduced distance between the devices on a chip and the use of thin-film MIM capacitors with high capacitance density.

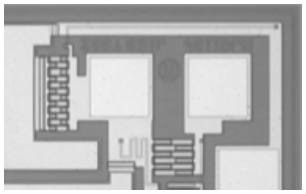

Figure 9: Photograph of the ESD protection device in DTV LNA

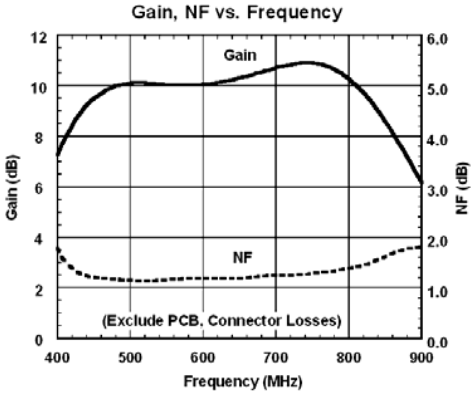

Figure 10: Gain and NF characteristics of DTV LNA

TABLE 2: Performance of DTV LNA

High- gain mode (LNA mode)	Low- gain mode (bypass mode)
IDD=4 mA	IDD=10 uA
Gain=10 dB	Gain=- 0.6 dB
NF=1.2 dB	-
IIP3=+5 dBm	IIP3=+23 dBm
P- 1dB (IN)=- 5 dBm	P- 1dB (IN)=+4 dBm

CONCLUSIONS

An advanced fabrication process for GaAs MMICs fitted with electrostatic-discharge (ESD) protection devices, which are formed on a wafer with E/D-mode HJFETs, was developed. This process is realized by using only one additional mask and two additional etching steps to the conventional process flow for production of HJFETs. Optimizing the epi-structure of PIN diodes and selecting appropriate ESD protection device size makes it possible to realize high ESD tolerance and high RF performance simultaneously. A high-performance SW and LNA MMICs fabricated by this new process were confirmed to maintain high ESD tolerance.

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ACRONYMS

GaAs: Gallium Arsenide
MMIC: Microwave Monolithic Integrated Circuit
ESD: Electrostatic Discharge
HJFET: Hetero-Junction Field-Effect Transistor
AlGaAs: Aluminum Gallium Arsenide
InGaAs: Indium Gallium Arsenide
InGaP: Indium Gallium Phosphide
DP7T: Double-Pole 7-Throw