Self Aligned Field-Plate PHEMT for 5.8 GHz Operation

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INTRODUCTION

GaAs PHEMT's have been the workhorse for microwave discretes and MMIC's for many years. Freescale Semiconductor has participated in this market for applications up to 3.55GHz using a backfilled gate process for devices with an operating voltage of 12V. We have also reported a number of enhancements to this device technology in the technical literature [1-2]. This paper reports on work to take this technology to the next level by achieving CW and ACPR performance at 5.8 GHz which is equivalent to the performance at 3.55 GHz [3]. The use of a self-aligned field-plate was necessary to achieve RF gain > 10 dB while meeting all of the other performance targets with the same input match. This paper will review the epi structure, process, and device design that enabled this performance increase.

DEVICE DESIGN CONSIDERATIONS

Using device simulation to optimize the device design space and pizza mask experimentation the following device design parameters were investigated: L_{sg}, L_{dg}, L_g, gate-gate pitch, Z_f (individual gate finger length), Z_T (total gate periphery), T-gate cross-section, slot source vias, air bridges, and field-plate resistance. In some cases these changes produced the expected response and in others they did not. However in the end two device designs enabled the desired performance improvements.

FABRICATION

The key process feature that enabled this performance improvement at 5.8 GHz was the use of Freescale's self-aligned field-plate process. The major fabrication steps are outlined here, and illustrated in Figure 1. The first steps in the process involve etching the N^+ cap, achieving device isolation with ion implantation, and depositing the first dielectric layers on which the field-plate metal is deposited. Next the field-plate metal is defined and etched. The field-plate is covered with a second dielectric layer. Ohmic contacts are formed and annealed (not shown in illustration). The gate via is defined, and then etching is used to remove in succession the top dielectric, the field-plate metal that resides in the gate via opening, and the dielectric on which the field-plate metal is deposited. Next the spacer dielectric is deposited and removed everywhere except on the sidewalls of the gate via. A seed layer is deposited which is followed by selectively plating the gate metal. The device fabrication is completed (not shown in illustration) with deposition and patterning of interlayer dielectric, plating a thick second layer metal, passivation deposition, thinning the wafer to 1 mil, etching substrate via holes, and finally depositing a thick backmetal for packaging and mechanical stability.

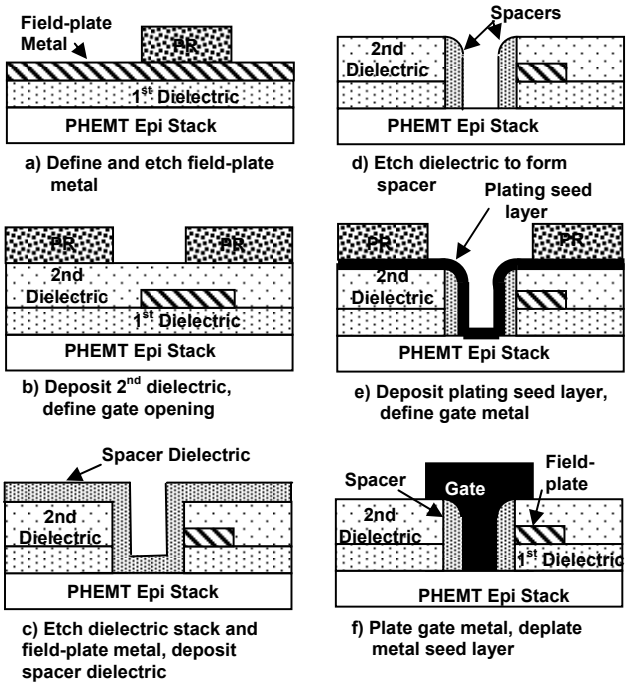

Figure 1: Process flow for fabrication of a self-aligned field plate PHEMT

An SEM cross-section of a completed device focused on the gate/field plate area is shown in Figure 2. The device shown has a drawn gate length of 0.7µm, a measured gate length of 0.4µm, a spacer length of 0.1µm, and a top-T gate length of 1.2µm.

DC DEVICE PARAMETERS

Figure 3 shows IV characteristic for 2.4mm unit cell with I_{DSS} = 500 mA and V_{GS} in -0.2 V steps. A variety of devices were studied at both PCM test (small, 2-finger devices) and

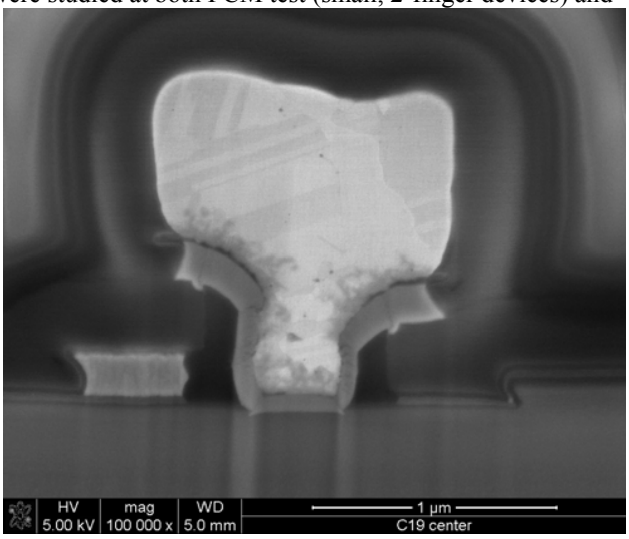

Figure 2: SEM cross-section of a GaAs PHEMT with self-aligned field plate. Drawn gate length is 0.7µm, physical gate length is 0.4µm.

unit probe (up to 18mm devices), in order to better understand the device design tradeoffs. Typical PCM results for a 2x300µm finger device with Lg=0.4µm, Lgs=0.7µm, and Lgd=2.2µm are shown in Table 1. It should be noted that in addition to improving the RF gain of the PHEMT, as will be discussed later in this paper, the addition of the field plate to the flow also improves the DC breakdown voltage compared to the non-field plate device, typically by around 10V.

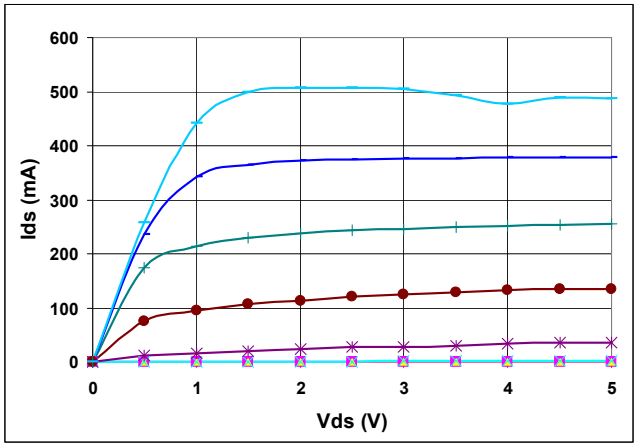

Fig 3. DC IV for 2.4mm PHEMT with I_{DSS} = 208 mA/mm with V_{GS} in - 0.2 V steps.

RF DEVICE PERFORMANCE

Small signal testing was performed on a variety of on-wafer probable structures, over several wafers, with several die per wafer per design tested. At shorter gate lengths, many of the non-field-plate designs failed at 12V. A typical

TABLE 1:
PCM DATA SUMMARY FOR FIELD PLATE PHEMT WITH 2X0.4X300MM GATE

Device Parameter	Average	Standard Deviation
Vth	-0.94 V	0.11 V
Ib (Vg=0)	209 mA/mm	19 mA/mm
Ids07 (Vg=+0.7V)	341 mA/mm	11 mA/mm
BVGS	22.8 V	1.5 V
BVGD	42.0 V	4.2 V

2.4mm field plate device with Lg=0.4µm, Lgs=0.7µm, and Lgd=2.6µm had f_t values around 14-15GHz, with small signal gain of 18.5-19.5dB at 5.8GHz. This high small signal gain at 5.8GHz demonstrates the large signal capability for this device at 5.8GHz. Figure 4 shows typical s-parameter data for the 2.4mm field plate device.

Across the wide range of designs tested under small signal conditions, a few consistent trends could be observed, some of which were unexpected. Shorter gates and longer gate-to-gate spacing improved small signal performance, and the presence of a field plate consistently improved gain. Unexpected results for this set of experiments included no apparent improvement from use of slot source vias instead of end source vias, or air bridges instead of dielectric crossovers.

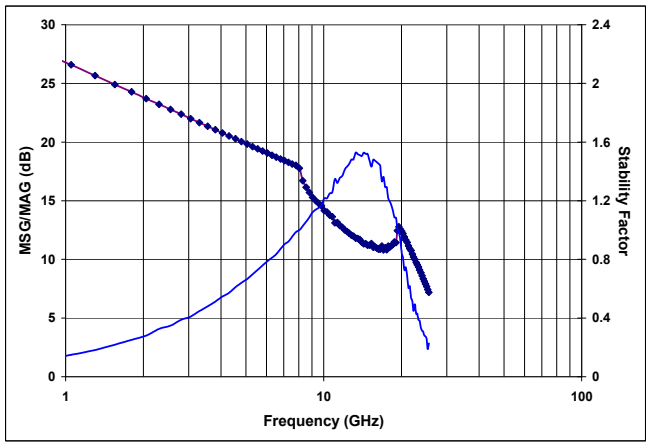

Figure 4: H21 vs. frequency for a 2.4mm field plate PHEMT with L_g=0.4µm, L_{gs}=0.7µm, and L_{gd}=2.6µm. Measurements were from 500MHz to 26.5GHz.

In order to compare the CW and W-CDMA performance of the different device designs under study, large gate

periphery (15-20mm) parts were assembled in ceramic packages for high frequency large-signal characterization.

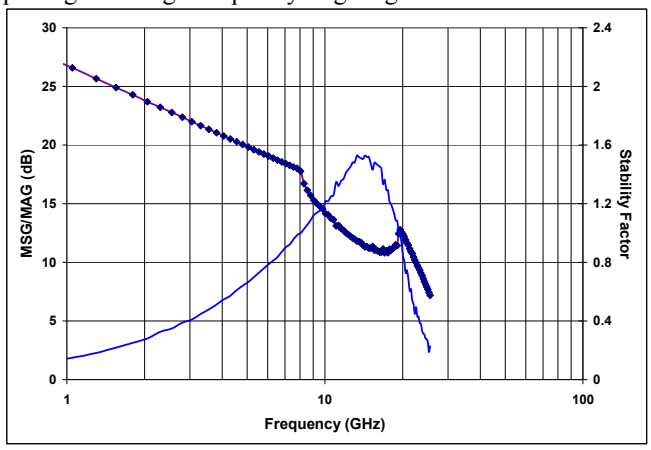

Figure 5: Small signal gain and stability vs. frequency for a 2.4mm field plate PHEMT with L_g=0.4µm, L_{gs}=0.7µm, and L_{gd}=2.6µm. Measurements were from 500MHz to 26.5GHz.

Figure 6 shows CW performance for a 19.2mm device with L_g=0.4µm, L_{gs}=0.7µm, and L_{gd}=2.6µm. This device, which was one of the two best performing designs, achieved 5.8GHz CW performance of P_{OUT} = 10 W, or 520mW/mm power density. The device gain was greater than 10 dB and IRL remained less than -10 dB. The CW PAE of this device was 46%. Linear performance is shown in Figure 7. The device achieves greater than 10 dB gain, with ACPR less than -40 dBc at 1 W P_{OUT}. This RF performance exceeded target specifications for the device, and exceeds the 5.8GHz performance of the current 10W discrete device by 0.5-1dB of P_{OUT} and 2-2.5dB of CW gain, while keeping other device performance characteristics to target. Table 2 shows a more detailed performance comparison of the 2 best designs from this experiment, as compared to the current 10W discrete. A number of other new designs without a field plate were also tested, but none of the non-field-plate designs were able to achieve the 10W CW gain and 40dBm P_{OUT} achieved by the field plate parts.

One of the interesting characteristics of the field plate device when studied under large signal conditions is that its tuning "tradeoffs" are radically different from the non-field-plate PHEMT. The field plate device has much higher gain—by several dB--but also tends to have somewhat degraded return loss and ACP characteristics as compared to the non-field-plate device. So, for the field plate device, it becomes necessary to tune away from optimal gain in order to achieve the required IRL and ACP. For the non-field-plate device, ACP and IRL are easy to achieve, so they are traded away in tuning in order to achieve maximum gain.

RELIABILITY

These PHEMT's are targeted for infrastructure/basestation applications, so reliability is of paramount importance. A typical reliability target would be a less than 10% change

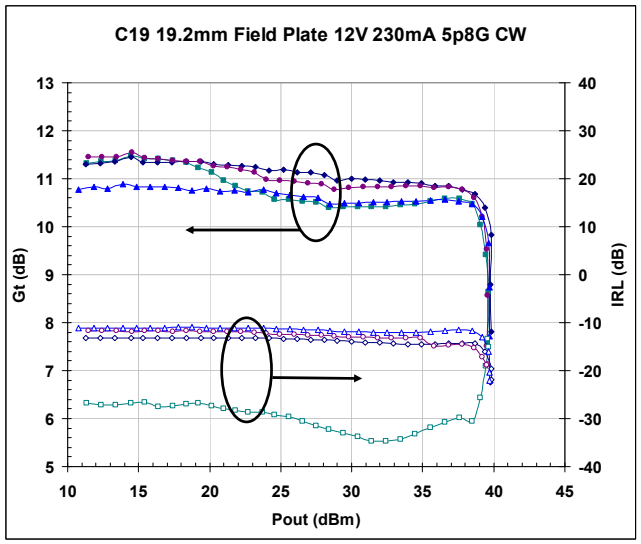

Figure 6: Continuous wave performance of 19.2mm field plate PHEMT with L_g=0.4µm, L_{gs}=0.7µm, and L_{gd}=2.6µm. CW gain, output power, and return loss at 5.8GHz are shown for a bias condition of V_{ds}=12V, I_{ds}=12mA/mm.

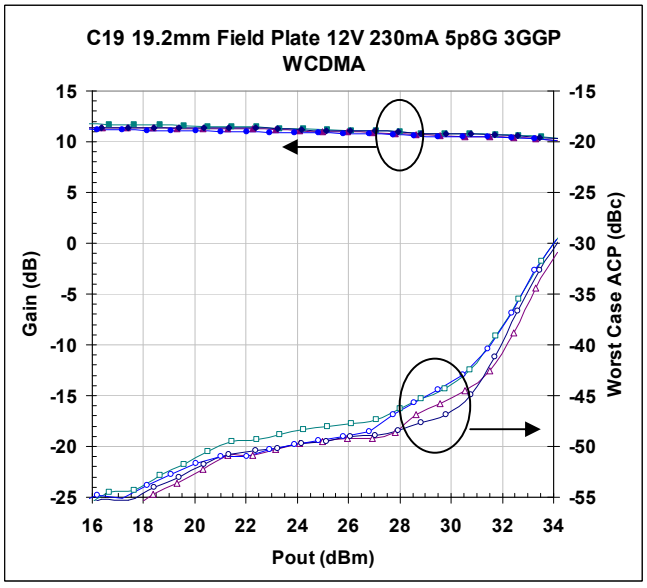

Figure 7: 5.8GHz Wideband CDMA performance of 19.2mm field plate PHEMT with L_g=0.4µm, L_{gs}=0.7µm, and L_{gd}=2.6µm. Gain and worst case ACP are shown for a bias condition of V_{ds}=12V, I_{ds}=12mA/mm.

over 20 years of operation. Step-stress reliability testing [4] was performed on the field plate PHEMT's. At bias conditions of V_{DS} = 12V and I_{DS} = 70 mA/mm, the MTTF was 4.2×10^6 hours and the activation energy was 1.49eV with $T_{CHANNEL}$ = 150°C. Reliability testing was performed on devices with both air bridge and conventional dielectric crossovers. As can be seen in Figures 8 and 9, there was no

statistically significant difference in the reliability performance of the devices with and without air bridges.

TABLE 2
5.8GHZ CW AND W-CDMA LARGE-SIGNAL PERFORMANCE OF 2 BEST NEW EXPERIMENTAL DESIGNS AND CURRENT 10W DISCRETE

Device	CW P_{out} (dBm)	CW Gain (dB)	Input Return Loss (dB)	P_{out} @ -40dBc ACP	ACPR @ -1.5dB backoff	W-CDMA Drain Efficiency (%)
Field Plate PHEMT "A"	40	10.5	-10	31.5	-44	24
Field Plate PHEMT "B"	39.5	10	-10	31.5	-44	25.5
Current 10W Discrete	39	8	-12	31.5	-44	25

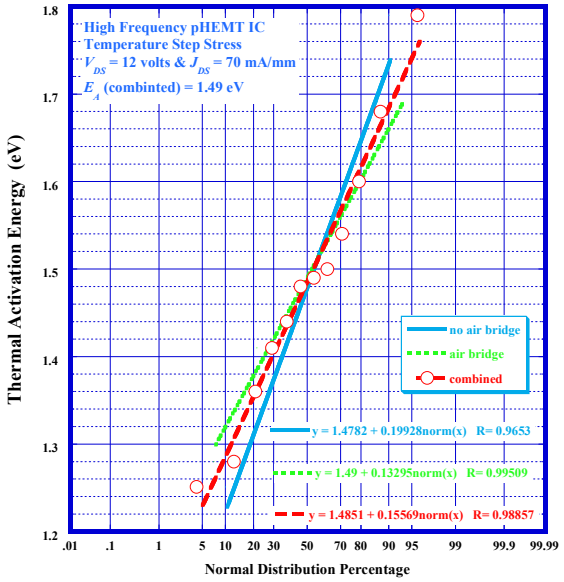

Figure 8: Thermal activation energy of a 0.4µm gate length field plate PHEMT, showing data for air bridge vs. no air bridge, and for all devices combined.

These data are comparable to reliability testing on earlier generation field plate PHEMT's with longer gate lengths, and to Freescale's commercially available (non-field plate) PHEMT product line.

CONCLUSIONS

We have demonstrated outstanding small signal, large signal, and linear performance at 5.8GHz in a GaAs PHEMT fabricated through the use of a self-aligned field plate. The use of the field plate brings significant advantages in breakdown voltage, and small- and large-signal gain. The reliability of the field plate PHEMT exceeds requirements for targeted infrastructure applications, and is comparable to its

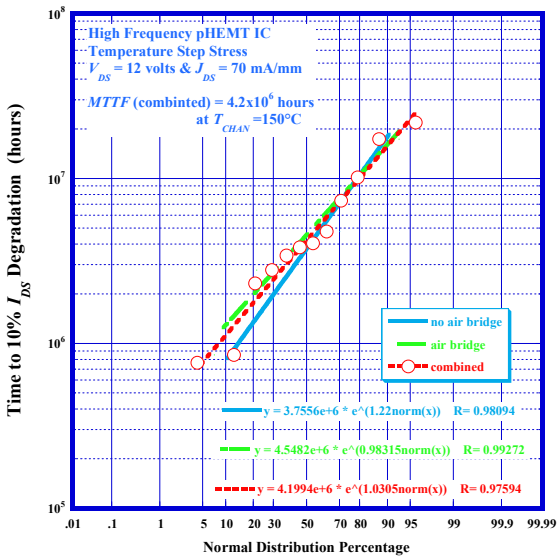

Figure 9: Mean time to failure, based on step stress testing, for a 0.4µm gate length field plate PHEMT, showing data for air bridge vs. no air bridge, and for all devices combined.

non-field plate predecessor that has been sold by Motorola/ Freescale for many years. The outstanding performance of the field plate PHEMT—40dBm Pout and better than 10dB CW gain, -10dB IRL, better than 10dB linear gain (W-CDMA), and -40dBc ACP at 1W output power—are the result of the simultaneous study and optimization of a large number of device design variables applied to a robust device integration.

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