150 nm InP HBT Process with Two-Level Airbridge Interconnects and MIM Capacitors for Sub-Millimeter Wave Research

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Keywords: Indium Phosphide, Heterojunction Bipolar Transistor, MMIC.

Abstract:

A 150 nm emitter width HBT fabrication process for device-level research is described. Simple passive elements are integrated after device planarization for future demonstration of sub-millimeter wave MMICs.

INTRODUCTION

InP transistors have the highest cutoff frequencies of any current transistor technology, but the limits of the material system have not yet been reached. InP HEMTs with 35 nm gate lengths have reported power gain cutoff frequencies (f_{MAX}) exceeding 1 THz [1]. We have reported vertically scaled InP SHBTs and DHBTs with current gain cutoff frequencies (f_T) as high as 765 GHz and 670 GHz [2, 3], respectively, using 0.3 – 0.5 μm emitter widths. While vertical scaling and energy band engineering successfully reduced the traditionally dominant electron transport delays in these InP HBTs, parasitic RC charging delays now represent 35-50% of total f_T delay in the vertically scaled devices having collector thicknesses < 1000 Å. The increasing base-collector junction capacitance and base resistance associated with vertical scaling lowers the power-gain cutoff frequency f_{MAX}. To offset the increasing significance of extrinsic parasitic RC charging delay, lateral (fabrication) scaling beyond the 0.25 μm node is needed. Equation (1) represents the HBT f_T delay as the sum of two transit and two RC charging terms. Here τ_B and τ_C are the base and collector transit times. R_E, and R_C are the total emitter and collector resistances, respectively. C_{JE} is the base-emitter junction capacitance and C_{BC} is the base-collector junction capacitance. The coefficient of C_{JE} is the dynamic resistance of the forward-biased emitter-base junction.

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{kT}{qI_C}C_{JE} + (R_C + R_E + \frac{kT}{qI_C})C_{BC} \qquad (1)$$

When f_T delay is equally partitioned between transit delay and charging delay, as we have shown for aggressively scaled devices, both types of delay must be targeted when scaling to increase cutoff frequency. The emitter width controls the intrinsic active area of the HBT and because of the top-down scaling nature of the traditional mesa-HBT, it also impacts the ability to scale the extrinsic parasitic resistances (R_B, R_C)

and capacitances (C_{BC}). Proportional scaling applied to the current highest cutoff frequency InP HBTs requires emitter widths < 200 nm to reach THz f_T and/or f_{MAX} [4].

150 NM HBT FABRICATION PROCESS

An existing sub-μm fabrication process [5] was modified to yield devices with 150-350 nm active area and to integrate passive MMIC elements. Table 1 outlines the modified process steps. The emitter contact is defined by 50 keV electron beam lithography using a tri-layer PMMA/PMGI/PMMA photoresist stack. The tri-layer resist allows for control of the critical dimension while retaining high aspect ratio > 3, necessary because the emitter ohmic metal is also a contact post. The emitter electrode has a narrow 'foot' corresponding to the lower photoresist layer with a slightly wider tapered 'head'. The emitter foot width is varied from 180 nm to 350 nm with corresponding emitter head widths of 276 nm to 450 nm after Ti/Pt/Au deposition

Table 1. Transistor and passive element fabrication process.

| Process Step	Description
1. Emitter Contact	E-beam lithography, e-beam evaporation of 500nm Ti/Pt/Au ohmic contact, liftoff.
2. Emitter Sidewall	90 nm PECVD SiN, 40 mTorr CF$_4$ RIE overetch to 40 nm spacer width.
3. Emitter Mesa Etch	Wet chemical etch, aligned to emitter sidewall, 40 nm lateral undercut.
4. Base Contact	E-beam lithography, e-beam evaporation of 50nm Ti/Pt/Au ohmic contact, liftoff.
5. Base-Collector Mesa Etch	45 nm PECVD SiN, e-beam lithography, thermal Al hardmask evaporation, liftoff. 40 mT CF$_4$ RIE, wet etch Al hardmask. Wet chemical etch, aligned to base contact, 50-150 nm lateral undercut.
6. Collector Contact	E-beam lithography, e-beam evaporation of 250nm Ti/Pt/Au ohmic contact, liftoff
7. Post Metal	E-beam lithography, e-beam evaporation of 750 nm Ti/Au.
8. Isolation Etch	I-line lithography, wet chemical etch to SI substrate. Base post airbridge released.
9. Planarization	Spin coat, cure BCB. 50 mTorr CF$_4$ RIE to expose posts.
10. NiCr TFR	I-line lithography, thermal evaporation 25 nm NiCr.
11. Metal 1	I-line lithography, e-beam evaporation of 1000 nm Ti/Au.
12. Capacitor Dielectric / Via	170 nm PECVD SiN. I-line lithography, 50 mTorr CF$_4$ RIE.
13. Airbridge Formation	I-line lithography, sacrificial resist reflow bake, e-beam evaporation of Ni interlayer.
14. Metal 2	I-line lithography, wet chemical Ni interlayer etch, e-beam evaporation of 2000 nm Ti/Au.
15. Airbridge Release	Wet chemical Ni interlayer etch, dissolve sacrificial resist.
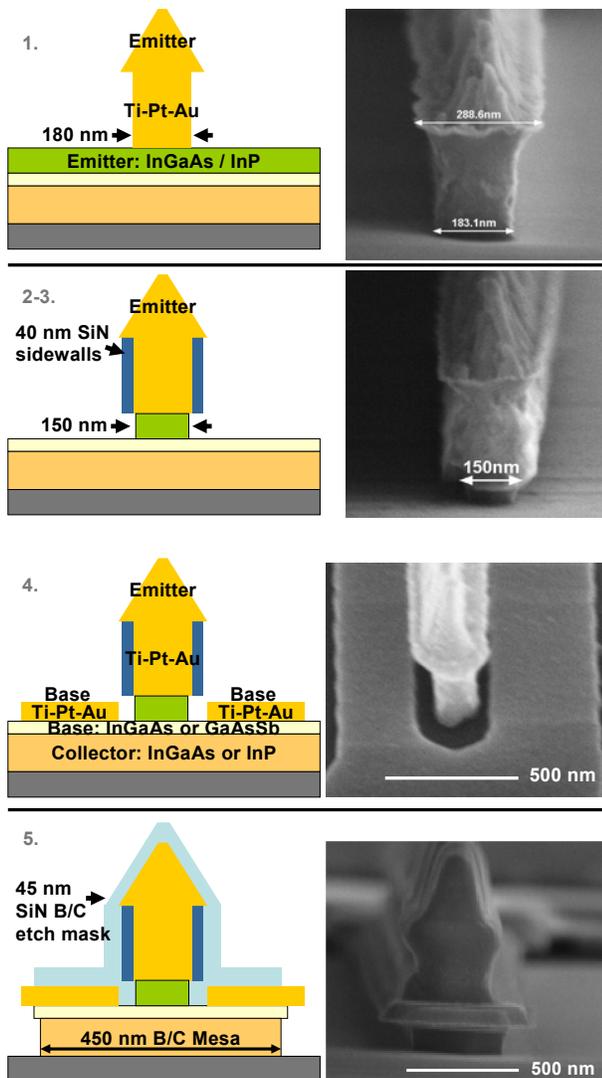
Figure 1. Illustrations and SEM images of key fabrication steps defining the transistor active area. Numbered sections correspond to steps listed in Table 1.

by electron beam evaporation and liftoff. Emitter lengths are varied from 1-8 µm. A sidewall spacer is created around the emitter foot by conformal PECVD silicon nitride, etched back in an anisotropic low pressure CF$_4$ plasma. The 40 nm sidewall offsets the emitter cap wet chemical etch so that the emitter contact is not undercut, which would increase emitter resistance. After the emitter mesa etch, the self-aligned base ohmic contact is defined by EBL and Ti/Pt/Au electron beam evaporation. The base contact to emitter spacing is controlled by the emitter head-to-foot width offset. To self-align the base-collector mesa etch to the base contact edge, the active area is protected by a 45 nm PECVD silicon nitride layer. EBL is used to define an aluminum hardmask pattern just inside the dimensions of the base contact, and this is transferred to the nitride using CF$_4$ RIE. The outside dimensions of the base contact width are varied from 550-

1050 nm to control the base-resistance / base-collector capacitance tradeoff. This dimension is further controlled by the wet chemical etch undercut of the base-collector mesa etch. This completes the definition of the device active area, and the key features of these process steps are illustrated in Fig. 1 which also shows SEM images of a minimum-sized device after each process step.

The devices are completed by deposition of a collector contact on the sub-collector layer, re-aligned by EBL. A final post metal step is required to bring the base and collector contact pads even with the emitter post height. The transistors are then protected by a standard I-line photoresist during the isolation wet etch down to the semi-insulating substrate. The isolation etch removes the material between the active device and the base post pad, creating a base metal airbridge and eliminating parasitic C_{BC} associated with the pad. The device after isolation is shown in an annotated SEM image in Fig. 2. Following the isolation, the devices are planarized in BCB. The BCB is etched back by CF$_4$ RIE to expose the transistor contact posts.
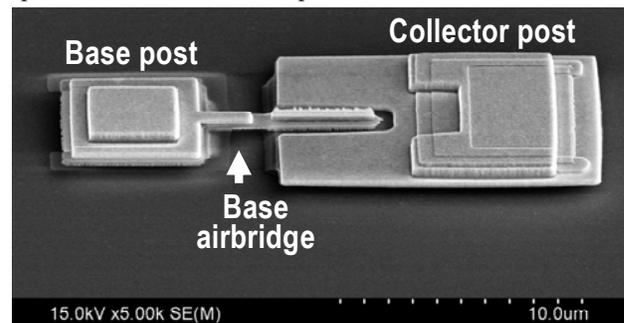

Figure 2. SEM image of complete transistor structure following isolation.

PASSIVE COMPONENT FABRICATION

NiCr thin film resistors are defined by thermal evaporation and liftoff. The 25 nm NiCr film thickness targets 50 Ω/□ sheet resistance. The resistors and exposed transistor contact posts are contacted by Metal 1, a 1 µm Ti/Au liftoff step that defines coplanar waveguides and MIM capacitor bottom layers. The capacitor dielectric is 170 nm PECVD silicon nitride. Vias through the nitride are formed by I-line lithography and CF$_4$ RIE. An airbridge process follows to form ground plane straps at discontinuities along the coplanar waveguides. PMGI photoresist is used as the airbridge sacrificial layer by first patterning with a standard I-line photoresist and then reflowing on a hotplate. The PMGI thickness is approximately 1.9 µm near the center of the airbridge structures after the reflow bake. A nickel interlayer is blanket deposited by electron beam evaporation to avoid exposing the sacrificial layer to subsequent photoresist application during Metal 2 patterning. Metal 2 defines the airbridge metal and MIM capacitor top layer. The nickel is etched through the Metal 2 photoresist windows prior to deposition and liftoff of 2 µm Ti/Au. Finally, the remaining nickel is stripped and the sacrificial PMGI dissolved in a NMP bath. Fig. 3 presents an SEM image of a two-stage

amplifier process test structure, showing various waveguide dimensions with airbridge ground plane straps and MIM capacitors for DC bias stubs and DC blocking between stages.
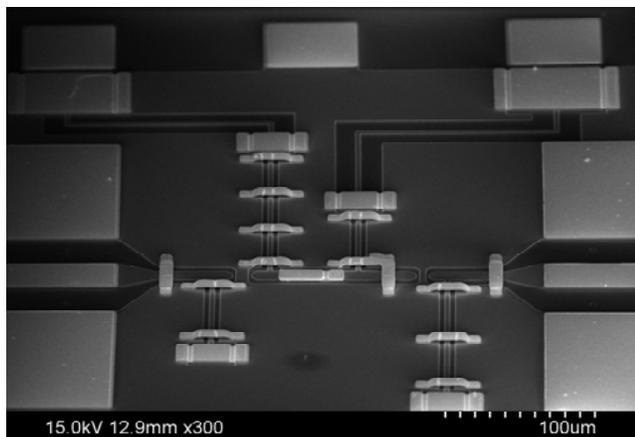

Figure 3. SEM image of two-stage power amplifier process test structure. MIM capacitors terminate matching and DC bias stubs. Airbridge ground plane straps suppress slot-line mode at discontinuities and lower ground path inductance.

MEASURED TRANSISTOR DATA

A pseudomorphic SHBT material structure was used to characterize the yield and parasistic properties of the revised fabrication process. The structure consists of a n-5×10^{16} cm^{-3} 120 nm collector and p-8×10^{19} 22 nm base linearly graded from $In_{0.48}Ga_{0.52}As$ at the emitter-base junction to $In_{0.66}Ga_{0.36}As$ at the collector-subcollector interface. The InP emitter layer is capped with a strained InGaAs cap layer for low contact resistance. Transistor S-parameters were measured from 0.5 to 50 GHz using an Agilent 8364B vector network analyzer. Off-wafer SOLT calibrations were used and measured on-wafer open and short probe pad parasitics were subsequently de-embedded from the measurements. A
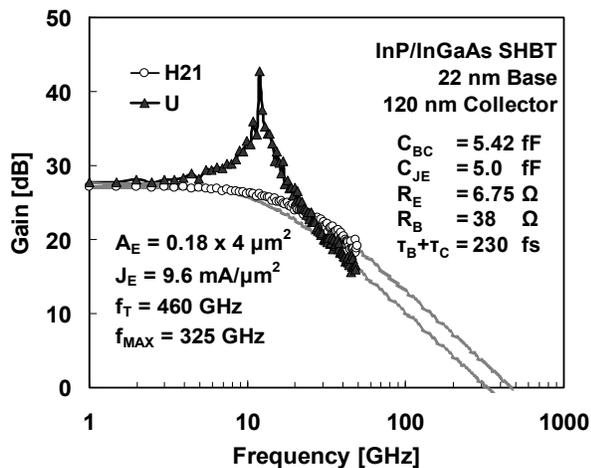
device with emitter dimensions 0.18×4 μm^2 achieves $f_T = 460$ GHz and simultaneous $f_{MAX} = 325$ GHz when operated at $J_E = 9.6$ mA/μm^2. Measured RF gain curves, extrapolations of f_T and f_{MAX}, and extracted delay term component values for the device are plotted in Fig. 4. The peaking of the power gain observed in Fig. 4 is expected for transistors having very small extrinsic C_{BC} and results from capacitance cancellation in the intrinsic collector depletion region when the transistor is under bias [6]. No device degradation attributed to the revised fabrication processes is observed in the RF characteristics of the devices. The specific contact resistance of the emitter is essentially constant at $\rho_{CE} = 4.9\text{-}5$ Ω-μm^2 across all emitter widths.

MEASURED PASSIVE ELEMENT DATA

The test mask processed in this work contains features such as isolated coplanar wave guide discontinuities and stub matching networks designed to verify small-signal models of these components to aid future circuit design efforts. The majority these elements are designed for > 300 GHz operation and are electrically small at the 50 GHz measurements obtained thus far. 50 GHz data for transmission line and for MIM capacitor test structures is presented here. The substrate consists of the full 625 μm SI InP wafer thickness coated with 1.2 μm BCB. The waveguide and capacitor bottom layer is 1 μm Au. The capacitor dielectric is 170 nm PECVD silicon nitride and the top layer metal is 2 μm Au.

Table 2 gives the measured 50 GHz characteristics of a 12 μm signal line width, 24 μm slot width coplanar waveguide. The parameters were extracted from measured S-parameters according to [7]. The measured parameters are in

Table 2. Electrical properties of 12μm-24μm CPW at 50 GHz.

R [Ω/mm]	L [nH/mm]	G [mS/mm]	C [pF/mm]	Z_0 [Ω]	$\varepsilon_{r,eff}$	Loss [dB/mm]
4.1	0.32	2.2	0.145	47	4.17	0.52

Figure 4. RF gain measurement and extrapolation of cutoff frequencies from initial device characterization using new fabrication process on 22nm base, 120 nm collector SHBT material structure.
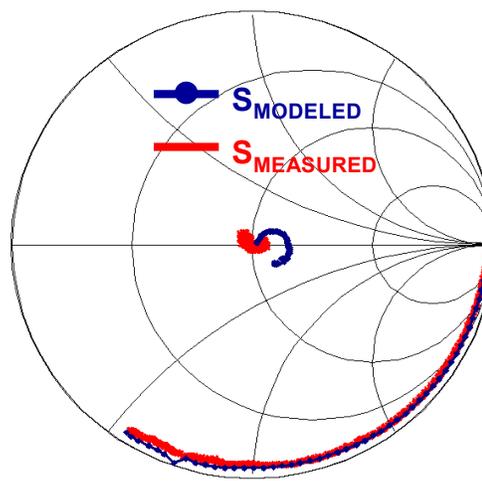

Figure 5. Measured and simulated S-parameters of 1 mm 12μm-24μm CPW from 500 MHz to 50 GHz.

good agreement with those simulated by 2.5-dimensional method of moments using Aglient ADS/Momentum software when the effects of the probe pads are removed by subtraction of on wafer short standard inductance and open standard capacitance. A comparison of the simulated and measured S-parameters over the full measured frequency range is shown in Fig. 5.

Table 3 gives typical measured parameters of MIM capacitor test structures. Less than 2% cross-wafer variation was observed for each parameter for a given capacitor size. All measured capacitors showed no significant leakage current when biased up to 40 V (limit of test setup).

Table 2. Electrical properties of MIM capacitor test structures.

Area [μm^2]	C [$pF/\mu m^2$]	Quality Factor (50 GHz)
45x45	3.59	11.9
55x55	3.40	11.1

$t_{SiN} = 175$ nm $\varepsilon_r \approx 7.1$

CONCLUSIONS

A method for producing InP HBTs with emitter widths ≤ 150 nm with minimal use of wet-etch undercut was demonstrated with sufficient yield for device-level research. Integration of MMIC passive elements opens up the potential for fabrication of sub-mm wave demonstration circuits using these aggressively scaled devices, but higher frequency models of the passive components need to be developed and verified.

REFERENCES
[1] R. Lai, et al., Proceedings of the 2007 IEEE International Electron Devices Meeting, 609 (2007).
[2] W. Snodgrass, et al., Proceedings of the 2006 IEEE International Electron Devices Meeting, 22.1.1 (2006).
[3] W. Snodgrass, et al., Proceedings of the 2007 IEEE International Electron Devices Meeting, 663 (2007).
[4] W. Snodgrass, et al., 2008 CS MANTECH Digest of Papers, 14.2 (2008).
[5] M. L. Hattendorf, et al., 2002 GaAs MANTECH Conference Digest of Papers, 255 (2002).
[6] M. Rohner, et al., IEEE Transactions on Electron Devices, **49**, 213 (2002).
[7] W. R. Eisenstadt, et al., Components, Hybrids, and Manufacturing Technology, IEEE Transactions on, **15**, 483 (1992).

ACRONYMS
BCB: bisbenzocyclobutene
CPW: Co-planar waveguide
DHBT: Double Heterojunction Bipolar Transistor
HBT: Heterojunction Bipolar Transistor
f_T: Currrent gain cutoff frequency
f_{MAX}: Power gain cutoff frequency
MIM: Metal-insulator-metal
MMIC: Monolithic microwave integrated circuit
PECVD: Plasma-enhanced chemical vapor deposition
RIE: Reactive-ion etching
SHBT: Single Heterojunction Bipolar Transistor
SI: Semi-insulating
SOLT: Short-Open-Load-Through