Investigating the ESD Robustness of RF Circuits and Elements by Transmission Line Pulsing

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Abstract

This work describes the application of a combined RF-TLP test set-up. It alternates between pulsed high current characterization and scattering parameter measurements up to 10 GHz in order to investigate the influence of the stress pulses on the RF behavior of the DUT. As an example, the high current behavior of a broad band amplifier circuit is analyzed. Furthermore the breakdown behavior of MIM capacitors fabricated in a GaAs technology is investigated.

INTRODUCTION

In order to investigate the robustness of integrated circuits against Electrostatic Discharge (ESD) it is necessary to access the high current behaviour of these devices. Transmission Line Pulsing (TLP) [1] is a well-established tool to analyze the elements and circuits in the ESD relevant time and current domain. In order to detect the failure threshold of the DUT (Device Under Test), an appropriate failure criterion has to be defined. For low frequency applications the leakage current at the stressed pin is a sensitive parameter to detect changes within the DUT. Melted junctions or broken gates lead to an increase of the DC current consumption. For RF applications, however, this is not necessarily the case. Matching networks at the I/O pads show inherently a higher current consumption depending on their impedance. This would hide a little increase of the current caused by the breakdown of a junction or a gate. Thus, it is essential to access also the RF parameters of the circuit after each stress pulse in order to detect the failure threshold of the DUT. To assure a proper S-parameter (scattering parameter) measurement by a vector network analyzer (VNA) on wafer level the RF-probes must permanently contact the measurement pads. This requires a decoupling between the VNA measurement loop and the TLP loop in order to guarantee a defined stress path. A first attempt to solve this problem is described in [2] where DC blocks are partly used to achieve this decoupling. However, TLP pulses are transient events. Depending on their rise time and pulse width DC blocks may not really decouple the pulses leading to unintended stress paths on the chip. In the following an alternative set-up is described, which applies SPDT (Single Pole Double Throw) switches.

MEASUREMENT SET UP

Figure 1 shows the RF-TLP measurement set-up [3, 4]. The TLP generator consists of a transmission line TL1 (impedance 50 Ohm) which is charged by the high voltage source V_{HV} on a defined pre-charge voltage. The length of this transmission line determines the pulse duration which can be varied from 100 ns down to a few nanoseconds. If the switch S_1 is closed, TL1 discharges producing a rectangular voltage pulse which passes the transmission lines TL2 and TL3. Depending on the impedance of the DUT the signal is reflected back into the system. From the incident and this reflected pulse the voltage across and the current through the DUT are calculated. By stepwise increasing the pulse amplitude a complete high current characteristic is obtained. By activating the appropriate SPDT switches the system monitors after each stress pulse various parameters of the DUT. SMU 1/2 measure the leakage current at the stress pin and the current consumption at the VDD pin, respectively. In addition the VNA measures the S-parameters which are compared with the pre-stress behaviour of the DUT. Beside the stress pin also all other pads of the circuit are connected via RF-SPDT switches, which ensures a defined stress and measurement path. However, the connection between the switches and the RF probe should be kept as short as possible in order to minimize the capacitive load at the involved pads. TL3 can be connected to each SPDT switch at the DUT pads allowing various stress combinations.

With this set-up it is possible to stress versus VSS/GND. In order to allow also stress combinations versus VDD or I/O it is necessary to disconnect the ground of TL3 from the SPDT switch and connect it separately to the desired stress ground terminal of the DUT.

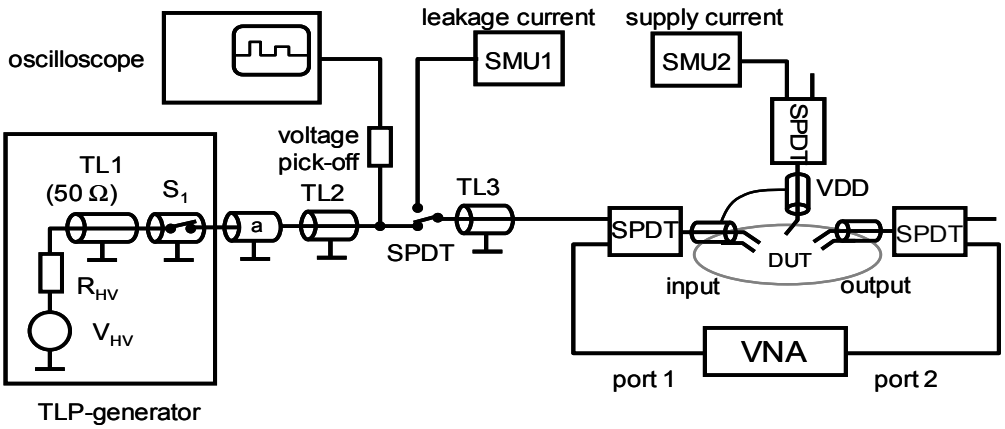

Figure 1: Measurement set-up of the RF-TLP system

INVESTIGATED BBLNA AND TEST RESULTS

As a first test circuit an RF-ESD co-designed broadband low noise amplifier (BB-LNA) as published in [4] was investigated. It was developed in a 130 nm CMOS process and applies three transistor stages with feedback circuit to provide bandwidth enhancement and bias. The lack of an AC input coupling capacitor brings a thin gate oxide (2.2 nm) directly to the IO node and allows in this case the emulation of a worst case product situation.

Three different low-C ESD protection concepts were realized: a) dual diode concept, b) bipolar elements and c) a transient triggered silicon controlled rectifier (TT-SCR) circuit.

The BBLNA has a measured gain of 10.9 dB (see fig. 2) and a (open deembedded) 3 dB bandwidth of about 5.7 GHz. This is in good accordance to simulation for the actual process corner identified by PCM data. For simulation a detailed parasitic extraction of the layout was performed. As expected, the performance loss due to ESD parasitics

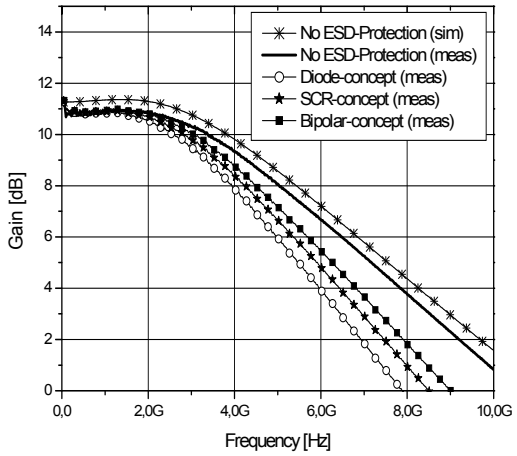

Fig. 2: RF performance of the unprotected and protected broadband LNA.

increases with frequency. At 5 GHz we find -2.1 dB for the diode and -1.4 dB for the TT-SCR concept. The TT-SCR protection provides an optimum concerning ESD protection level and RF performance of broad band GHz interfaces as far as reported in literature [5, 6].

As an example figure 3 shows the high current characteristic of the investigated BBLNA input versus ground with a SCR protection. The trigger voltage of the protection is 3.2 V, snapping back to a holding voltage of 1.5 V. The circuit fails at 2.1 A.

Figure 4 depicts the DC-characteristic of the failed device in comparison with the pre-stress characteristic.

It shows only a marginal increase of the leakage current for the failed device compared with the pre-stress leakage current which is caused by a matching circuit. This makes it difficult to use these data for failure detection. However, looking at the S21 parameter (fig. 5) a distinct drop of the gain from 10.9 dB to 7.5 dB can be observed. This is a clear indication for the failure of the device

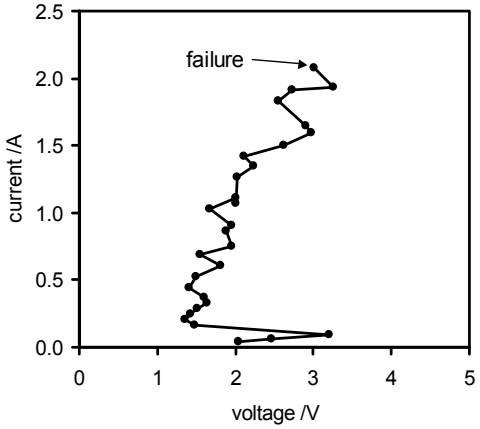

Fig. 3: High current behaviour of the BBLNA input with the SCR protection.

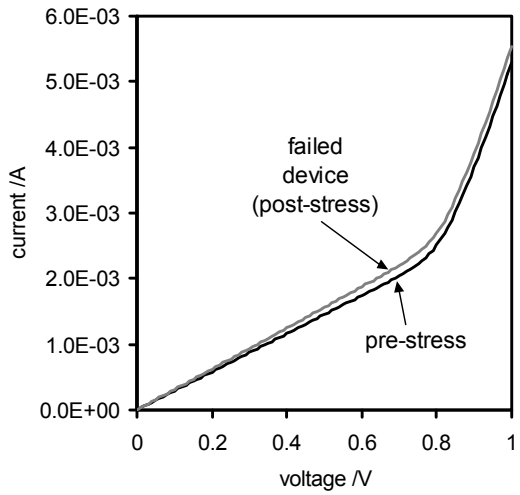

Fig. 4: Pre- and post-stress DC-characteristic of the BBLNA input with the SCR protection.

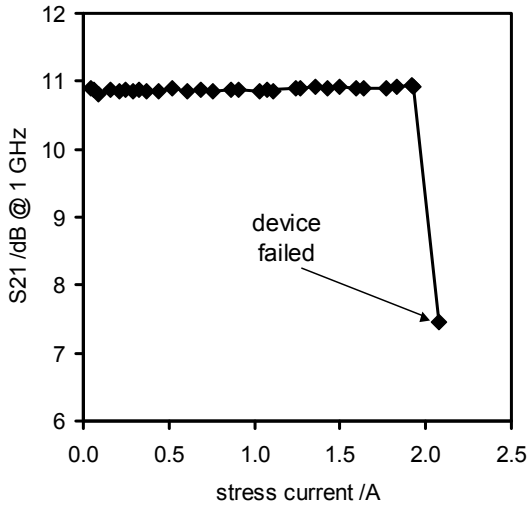

Fig. 5: S21 parameter measured at 1 GHz as function of the stress current.

This example shows that it might not be sufficient to apply the leakage current as failure criterion for high speed circuits. In addition, the S-parameters have to be taken into account in order to detect the failure threshold of the DUT.

INVESTIGATED MIM CAPACITORS AND TEST RESULTS

In a second example the breakdown behavior of MIM capacitors fabricated in a GaAs technology was investigated. For the measurement several sizes of capacitances have been available. To illustrate the different geometry of the investigated capacitors, figure 6 depicts the largest capacitor with a width of 300 µm -showing a typical damage spot- and as an insert the smallest capacitor with a width of 20 µm (without visible damage), drawn to scale for comparison.

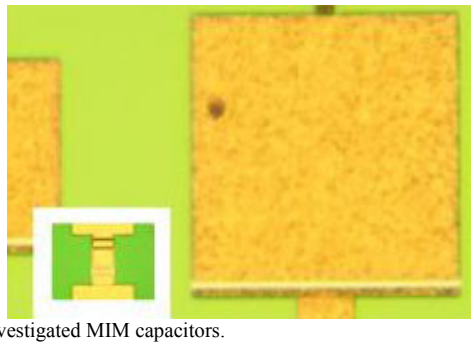

Fig. 6: Investigated MIM capacitors.

The breakdown behavior of these structures was investigated by TLP with two different pulse widths. In each case 3 devices per capacitor width have been stressed.
Figure 7 depicts the breakdown voltage as function of the device width for stress pulse width of 100 ns. It shows that the device width does not influence the breakdown voltage.

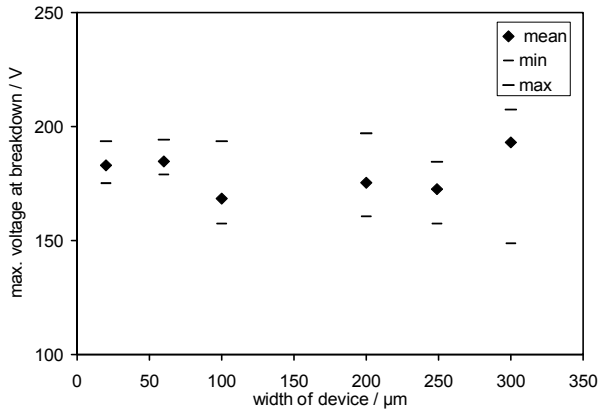

Fig. 7: Breakdown voltages of MIM capacitor structures for 100 ns TLP.

The mean value of the breakdown voltage for all devices is 180 V.
In order to investigate the breakdown also at a very short time scale, a pulse width of 1.5 ns was applied. Figure 8 shows the corresponding results.

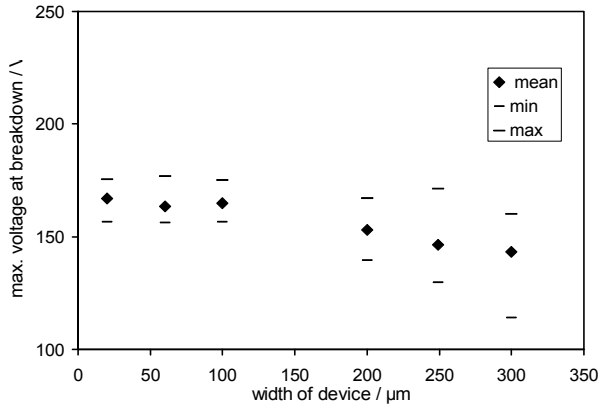

Fig. 8: Breakdown voltages of MIM capacitor structures for 1.5 ns TLP.

The data show, that the breakdown voltage slightly decreases with increasing device width. Furthermore, the mean value of the breakdown voltage for all devices is 160 V, which is below the result of the 100 ns pulse stress. A possible explanation for this unexpected behavior could be related to the different rise time of the 100 ns and the 1.5 ns stress pulses. The rise time of the 100 ns pulses is a few nanoseconds which addresses the time domain of the ESD stress model HBM. The 1.5 ns pulses address the time domain of the CDM and thus show a rise time of 200 ps. This leads to higher charging currents during the rising edge of the pulse and in turn this could lead to a localized high field strength exceeding a critical value.

In order to compare also the physical failure signatures a failure analysis was performed. Figure 9 shows as an example the result for the smallest device after removal of the top layer metal.

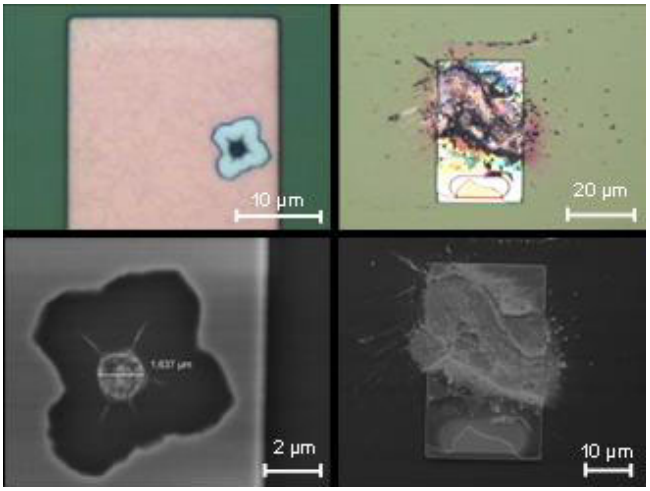

Fig. 9: Failure signatures after 1.5 ns pulse stress (left) and 100 ns pulse stress (right).

It shows on the left side the failure signature after 1.5 ns pulse stress and on the right side the damage after 100 ns pulse stress. The upper line shows the optical image and the lower line depicts the SEM image.

After 1.5 ns pulse stress the signature shows only a much localized damage, which is even not visible without removing the top layer metal.

After 100 ns pulse stress the complete device is damaged since the pulse energy is much higher.

The analysis of the physical failure signature helps to identify the possible root cause of failures observed in the field by assigning the damage to the appropriate time domain (eg. HBM or CDM).

CONCLUSIONS

A TLP set up is described, which also allows the investigation of RF elements and circuits. S-parameters are monitored after each stress pulse allowing sensitive failure detection. Moreover the application of RF SPDT switches at the terminals of the DUT ensures defined stress paths. The stress combinations versus VDD or I/O require a disruption of the 50 Ω environment which limits the minimum applicable stress pulse duration. The system is successfully applied to a broad band LNA circuit, which showed only a weak leakage current increase after TLP stressing. By evaluation the S-parameters the failure threshold could be clearly identified

In a second application the system was used to investigate the ESD susceptibility of MIM capacitors fabricated in a GaAs technology. The results of the failure analysis lead to the set up of a failure catalogue which can be applied to identify a possible root cause of field failures.

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ACRONYMS

BBLNA: Broad Band Low Noise Amplifier
CDM: Charged Device Model
DUT: Device Under Test
ESD: Electrostatic Discharge
HBM: Human Body Model
MIM: Metal Insulator Metal
RF: Radio Frequency
SPDT: Single Pole Double Throw
TLP: Transmission Line Pulser
TL: Transmission Line
TT-SCR:Transient Triggered Silicon Controlled Rectifier
VNA: Vector Network Analyzer