Wide Bandgap GaN Smart Power Chip Technology

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Abstract

Smart power chip technology has been realized on the GaN-on-Si platform, featuring monolithically integrated power devices, digital and analog functional blocks. In particular, this paper presents the imperative analog functional block – the voltage reference generator for smart power applications with wide-temperature-range stability. These circuits are shown to be capable of proper functions from room temperature up to 250 °C. The optimized voltage reference generator achieved less than 70 ppm/°C drift. It can be used to create a reference voltage for various biasing and sensing circuits.

Introduction

GaN-based power devices can be operated at high voltage and high current levels with high switching frequencies, and their inherent high-temperature operating capability could significantly reduce the burden for expensive cooling system used in advanced power converters. On the other hand, these devices do exhibit strong temperature-dependences as the intrinsic carrier mobility is affected by the temperature-sensitive phonon scattering. It is thus desirable to develop smart power chip technology with which we can implement on-chip power conditioning and protection circuits that promise to provide optimized performance, increased functionality and enhanced reliability. Up to now, based on a fluorine plasma ion implantation technology [1, 2], we have developed the key smart power components including high-voltage normally-off transistors and lateral field-effect rectifiers [3, 4]. We have also demonstrated the monolithic integration of enhancement-/depletion-mode AlGaN/GaN HEMTs for direct-coupled FET logic (DCFL) circuits that operate properly up to 375 °C [5, 6].

In this paper, we demonstrate a fundamental analog functional block, the voltage reference generator, on a proposed GaN smart power chip technology platform, as shown in Fig. 1. The voltage reference generators are essential for biasing circuits, analog-to-digital convertor and other sensing circuits. A voltage reference generator featuring one HEMT and four Schottky diode delivers voltage references with a drift less than 70 ppm/°C from room temperature to 250 °C.

GaN Smart Power Chip Technology Platform

The schematic cross section of the proposed platform for GaN smart power technology is shown in Fig. 1. To facilitate high integration density, a planar process [7] featuring isolation by fluorine plasma ion implantation is used to eliminate the 3D mesa formation. High voltage power devices and low voltage peripheral devices for mixed-signal functional blocks are fabricated on the same GaN-on-Si substrate with the same fabrication process.

The sample used in this work was a commercially

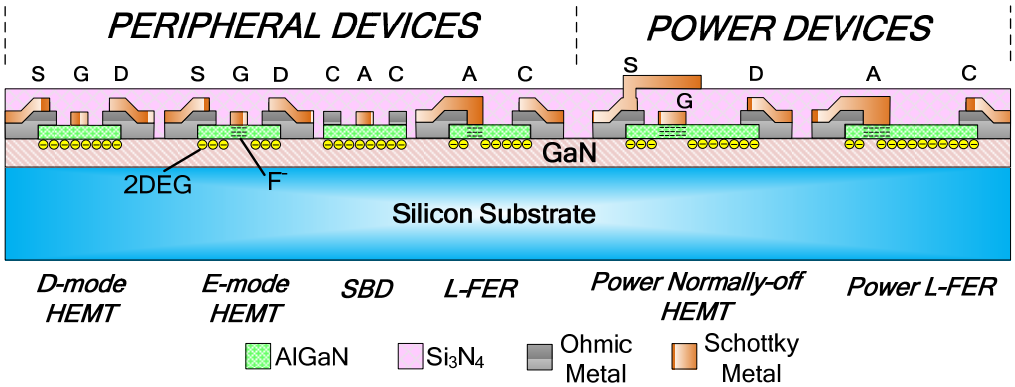

Fig. 1. Schematic platform of GaN smart power technology: integration of low-voltage peripheral and power devices.

available $Al_{0.26}Ga_{0.74}N$/GaN HEMT wafer grown by MOCVD on 4-inch silicon substrate. The epitaxial structure includes a GaN buffer, a thin AlN interface enhancement layer, 18 nm undoped AlGaN barrier and a 2nm GaN cap layer. The starting wafer featured a sheet resistance of 330 ohm/square, 2DEG mobility of 1800 $cm^2/V•s$ and a pinch off voltage of -2.1 V.

A. Power Devices

The fluorine plasma ion implantation (or treatment) technique, which was first reported in 2005 [2], is the key technology for the development of the power devices. The key feature is the incorporation of negatively charged fluorine ions under the Schottky gate that effectively depletes the 2DEG channel. Thus, the normally-off HEMT, which is required in the power electronics application, for its inherent fail-safe operation, can be realized. The robust control on the threshold voltage of the 2DEG channel is also recently utilized to realize a lateral field-effect rectifier (L-FER) that is completely compatible with normally-off HEMTs [3, 4].

Figure 2 plots the I-V characteristics of a normally-off AlGaN/GaN HEMT with a 1.5 µm gate-length and a 12 µm gate-drain distance. The device exhibits a threshold voltage (V_{th}) of 0.9 V, a maximum drain current (I_{max}) of 350 mA/mm at V_{GS}=3 V and V_{DS}=10 V, and a peak transconductance (G_m) of 175mA/mm. The off-state breakdown voltage is 370 V at a drain current leakage of 1 mA/mm and the specific on-resistance ($R_{ON, sp}$) is about 1.34 mΩ·cm^2 at V_{GS}=3 V.

The power rectifier L-FER with a cathode-to-anode drift length of 15 µm exhibits a breakdown voltage of 470 V, a low turn-on voltage of 0.58 V and a specific on-resistance of 2.04 mΩ.cm^2, as shown in Fig. 3. The $R_{ON,sp}$ versus breakdown voltage (*BV*) are summarized together with GaN-based rectifiers reported in the literatures in Fig. 3(c). Fig. 3 (d) compares the forward turn-on voltages ($V_{F, ON}$) of the L-FERs with other GaN-based rectifiers. The L-FERs exhibit significantly lower $V_{F, ON}$ than the vertical SBDs and p-i-n rectifiers. This is attributed to the L-FER's turn-on control mechanism that is based on the threshold voltage of the 2DEG channel, instead of the built-in potentials in Schottky junctions or p-n junctions.

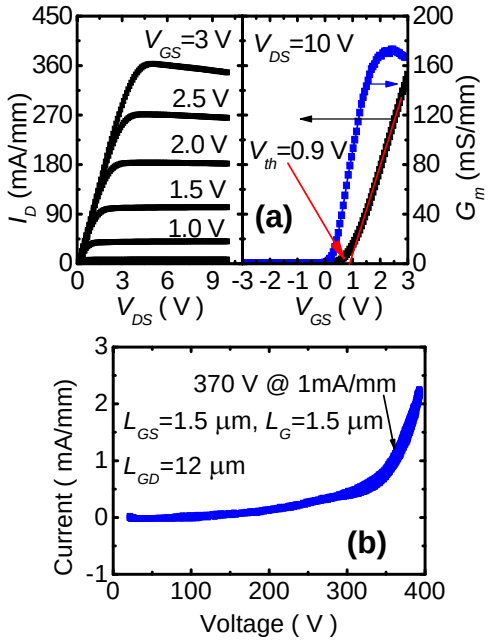

Fig. 2. Measured (a) on-state and (b) off-state characteristics of the normally-off HEMT with L_{GS}=1.5 µm, L_G=1.5 µm, and L_{GD}=12 µm.

B. Low-Voltage Devices

A smart power chip technology also requires low voltage peripheral devices for the implementation of digital and

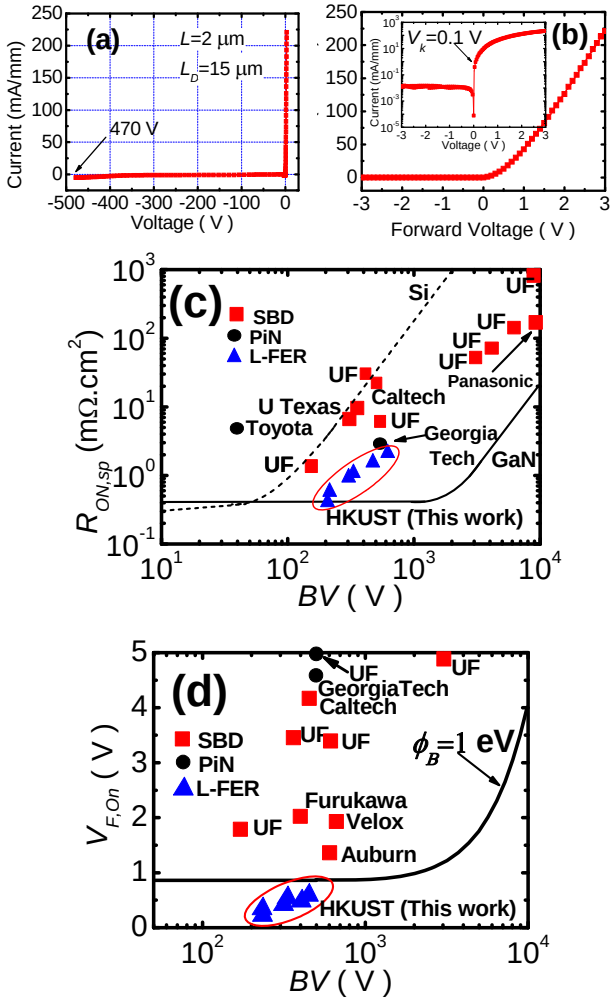

Fig. 3. Measured DC performances of L-FERs, (a) forward bias, (b) reverse bias, (c) The $R_{ON,sp}$ versus *BV* for GaN-based rectifiers reported in the literature. The dot and solid lines show the theoretical results for Si and GaN, respectively. (d) The $V_{F,ON}$ versus *BV* for GaN rectifiers. The curves shows theoretical values expected for barrier height of 1 eV.

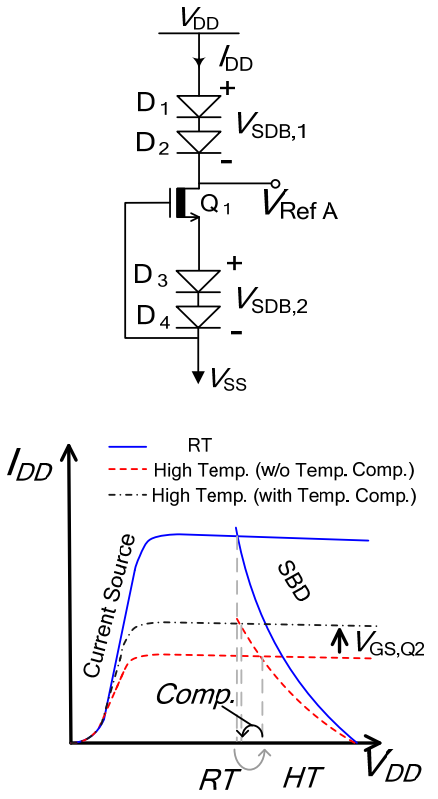

Fig. 4. Voltage reference generators with temperature and process compensation and the corresponding graphic analysis.

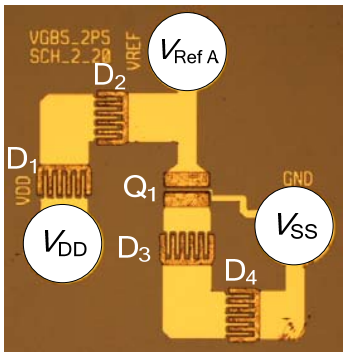

Fig. 5. Micro photo of the fabricated voltage reference.

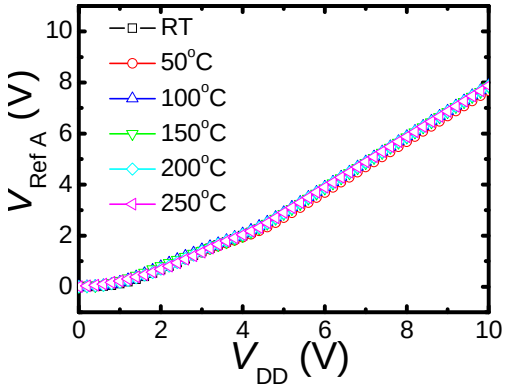

Fig. 6. Measured reference voltages of generator versus V_{DD} at different temperatures.

analog blocks. Due to the lack of high-performance p-channel GaN devices, the simplest circuit configuration for digital circuits is the direct-coupled FET logic (DCFL) that requires both the E-mode and D-mode HEMTs [2, 3]. The Schottky diodes and L-FERs all exhibits graceful temperature dependences that can be explored for temperature sensing and compensation.

GaN Voltage Reference Generators

A. Operating Principle

Figure 4 depicts the voltage reference circuit with temperature compensation [8] where gate voltage V_{GS} of HEMT Q_1 is varied as a function of the forward on-voltage of the series-connected SBDs D_3 and D_4. The current source with SBDs D_3 and D_4 degeneration in its source is designed, and the temperature variations of D_1 and D_2 can be compensated. For instance, as temperature rises, both the diode and HEMT features lower current level, and the output $V_{Ref\ A}$ tends to increase and the voltage drop across the SBDs ($V_{SDB,\,1}$ and $V_{SDB,\,2}$) will decrease. The decrease in $V_{SDB,\,2}$, in return results in a larger effective V_{GS} that tends to pull up the current and mitigate the rise in V_{Ref}. It should be noted that the potential drop across the degeneration SBDs must be smaller than the magnitude of the pinch off voltage of the HEMT to assure the turn-on of the transistor.

In our work, identical physical dimensions are used for the four SBDs featuring 5 pairs of metal fingers (2μm×20μm). The D-mode HEMT current source is designed with a gate length of 1.5 μm, a gate-source spacing of 1.5 μm, a gate-drain spacing of 2.5 μm, and a gate width of 50 μm, respectively. The micro graph of the fabricated voltage reference integrated circuit is shown in Fig. 5.

B. Experiments

The measured reference voltage versus supply voltage V_{DD} relationships at different temperature are shown in Fig. 6. The difference of V_{DD} and $V_{Ref\ A}$ becomes a constant when the current source HEMT operates in the saturation region. At room temperature, the starting operation point of the reference generator is V_{DD}= 4.3 V. At V_{DD} = 10 V, the supply current and power consumption of the reference generator are 0.8 mA and 8 mW, respectively. It should be noted that the power consumption can be reduced by further down-scaling of the device dimensions. As shown in Fig. 6, the generator has good high temperature robustness. From the graphic analysis described, both the current of the current source and SBD are decreased. However, V_{GS} of Q_1 is increased due to decreasing of the potential drop of the SBD pair. As a result, V_{Ref} drift can be compensated by using this

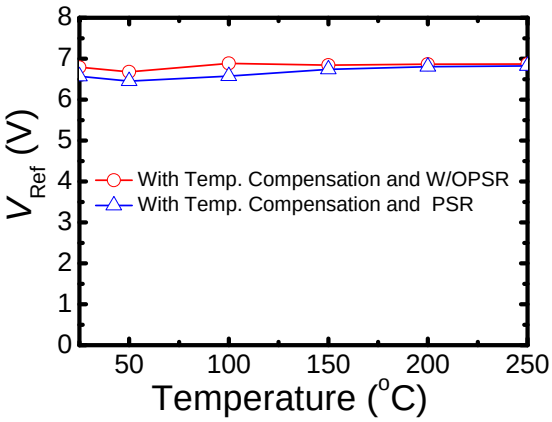

Fig. 7. Measured reference voltages of voltage reference generator as a function of temperatures at V_{DD}= 9 V.

feedback configuration. As shown in Fig. 7, at V_{DD} = 9 V, the output voltage variations of the voltage reference generator A achieved less than 70 ppm/^{o}C and a power supply rejection of 35 dB. It can be used as a reference voltage in various biasing and sensing circuits.

In smart power implementation, the sensing and control circuits are swamped with switching noise generated by the digital circuits and switch-mode power converters. To generate a reliable reference voltage in the harsh signal environment, the voltage reference must exhibit high dc accuracy despite supply noise. Figure 8 illustrates one design with ground noise rejection. The power supply rejection ratio (PSRR) is improved to 39 dB with the new design, showing a ~5dB improvement over that obtained in the original design (Fig. 4).

CONCLUSIONS

Smart power chip technology has been realized using the GaN-on-Si platform. The voltage reference generators for smart power applications with wide-temperature-range stability are demonstrated. These circuits are fabricated on standard GaN-on-Si AlGaN/GaN HEMT wafers are shown to be capable of proper operation from room temperature up to 250 ^{o}C. The voltage reference generator achieved less than 70 ppm/^{o}C drift and a 35 dB ground noise rejection ratio.

ACKNOWLEDGEMENTS

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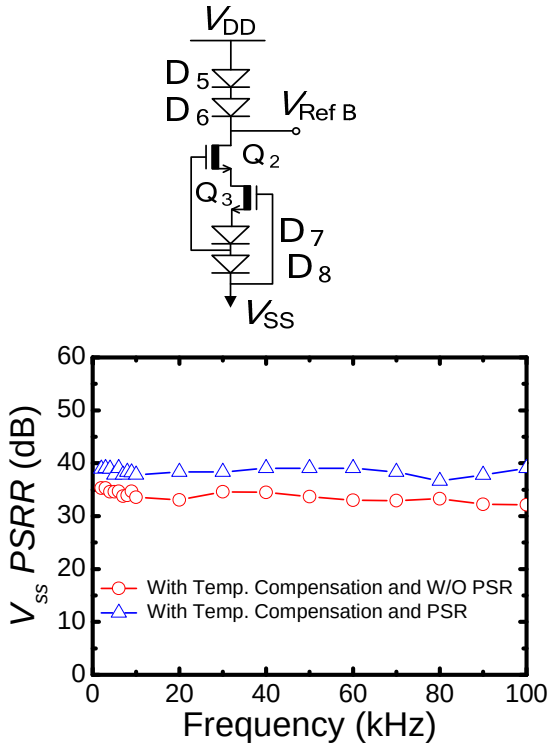

Fig. 8. Measured V_{SS} PSSR of voltage reference generator as a function of frequency at V_{DD}= 6 V.

ACRONYMS

DCFL: Direct-Coupled FET Logic
E/D-mode : Enhancement-/ Depletion-mode
HEMTs: High Electron Mobility Transistors
L-FER: Lateral Field Effect Rectifier
MOCVD: Metal-Organic Chemical Vapor Deposition
RTA: Rapid Thermal Annealing
SBD: Schottky Barrier Diode
2DEG: Two-Dimensional Electron Gas