Copper Interconnect on GaAs pHEMT by Evaporation Process

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Abstract

Copper (Cu) interconnects have been quite successful in Silicon micro-circuits but limited in compound semiconductor fabrication. Low resistivity, inertness to most wet chemicals and suitability for wire bonding are the reasons that Gold (Au) has remained the metal of choice for forming interconnects in the compound semiconductor industry. However, the prices of precious metals have risen steadily in the last two years driving the wafer cost up with it. Most development work being done on a Cu metal scheme suitable for compound semiconductor focuses on electroplating adopted from the matured Silicon processes. Recently Skyworks has successfully developed an evaporated Cu process; replacing Au in Metal 1 of our pHEMT process. In addition to lower wafer cost, evaporated Cu offers other technical advantages such as lower resistivity and reduced likelihood of spitting at high deposition rates. We will discuss the challenges in the development work. A comparison of DC and RF test parameters between wafers that have Au and Cu interconnects as well as reliability data will be presented

INTRODUCTION

Wafer cost is an important metric that measures the profitability and success of a semiconductor fab. Precious metal represents a substantial portion of a completed GaAs wafer cost. Gold (Au) and Platinum (Pt) have market prices that fluctuate with the demand. The current economic situation has driven the price of Au and Pt up steadily over the last couple of years. Although the precious metals prices are beyond one's control, with proper engineering, they can be replaced by a less expensive alternative.

The Metal 1 of a typical GaAs pHEMT has a thickness from 2 to 3 microns of Au. Depending on the design, the metallized area can range from 20 to 40%. Many attempts to find a substitute for Au focus on Copper (Cu). The choice is logical. Cu has a bulk resistivity (ρ) of 1.7 μOhm-cm; about 20% less than Au, which has a ρ of 2.2 μOhm-cm. 5N Cu slug suitable for evaporation is a fraction of the cost of Au slug of the same purity.

However, there are a few short comings with Cu. It is easily oxidized in air and it readily reacts with many wet chemistries commonly used in GaAs processing including HCl, NH_4OH and H_2O_2. Even NMP based resist stripper can attack Cu if certain additives are present in the solution. Furthermore, we have to take into consideration the potential effects Cu has on a GaAs device. If allowed to diffuse into the semiconductor, it will act as a trap rendering the device useless or adversely affecting long term reliability. [1], [2].

Cu interconnects on GaAs devices are still in the development stage. Most current work on a Cu metal scheme compatible with GaAs devices evolves around electro-plating borrowed from the matured Si processes [3], [4]. Cu plating with Chemical Mechanical Polishing (CMP) has been the standard Si process for making interconnect for a number of years. [5], [6]. Recently, we have successfully fabricated several pHEMTs using an evaporation / liftoff process commonly used in the III-V industry.

Many reasons justified the choice of evaporation / liftoff process. First, the existing tool set used for depositing Ohmic and Gate metal can be set up to run Cu. Second, evaporated Cu Metal1 does not require the additional wet steps of seed layer removal; whether it is de-plate or chemical etch. Finally, from a throughput consideration, Cu can be evaporated at high rates with minimal risk of spitting. As a result, for any given tool set, running Cu will have the higher throughput compared to Au.

Mainstream Cu electro-plating deposition rate is about 0.25 μm/min. Consider a four head plating cluster tool, a 2.5 μm interconnect would take about 60 minutes to process a 24 wafer lot. Evaporation done in a batch tool can usually hold 24 four inch wafers or more in a run. The throughput is comparable to the electro-plating process, but without the need for a separate sputtered seed layer step and a seed layer removal step.

The down side of evaporation is the limited choice of barrier metals. The sputtered seed layer can incorporate refractory metals and metal-nitrides; some of which are not suitable for E-beam evaporation due to the high melting point. Therefore electro-plating with a seed layer process offers a broad choice of materials including W, W-Ti or Ta, and their nitrides by reactive sputtering.

EXPERIMENTAL PROCEDURE

We selected a pHEMT switch mask with a large amount of historic data against which the experimental results can compare. The switches were built on an epi structure with an AlGaAs / InGaAs channel and a Si doped N+ cap layer. The wafers received our standard metal 1 photo process for liftoff. After which we deposited the Cu Metal 1 stack by E-beam evaporation.

Since Cu does not have a high tendency to spit in an E-beam evaporation process, a deposition rate of 15A/sec was chosen for the experiment. The deposition parameters, including the deposition rate, were determined based on film characteristics, throughput consideration and batch uniformity. All Cu metal 1 development work was done in a Temescal FCE2700 evaporator. We used a Tungsten (W) liner for Cu to lower the deposition power. The source was allowed plenty of cool time before venting to atmosphere. Otherwise Cu would quickly oxidize.

Our new generation of MMICs has tight performance specifications. To match the RF performance of the control wafer, a 20% thinner Cu layer was deposited so that the inductance of the circuit is not altered.

A final layer of Au / Ti cap, which served to protect the Cu from oxidizing, was deposited without breaking vacuum. The Ti layer was later etched away to expose the bond pads. This is necessary both for the probe needles to make good electrical contact as well as for wire bonding. Also included in the experiment were two control wafers. Other than the difference in the Metal 1 stack, the control wafers traveled with the rest of the lot throughout the process.

After a standard liftoff process, the wafers were cleaned of the remaining resist residue in NMP. An oxygen plasma descum step was then used to clean off any remaining organics before the wafers received the final nitride passivation.

Typical chemistries used in subsequent processes at this stage are either HCl or NH_4OH based. Either will attack Cu rapidly even in dilute concentration; typically at a location with poor step coverage where the Au / Ti cap can not conformally cover the Cu. Early attempts with standard pre-clean processes resulted in moderate Cu corrosion. See Fig [1]. For this reason, any step after Cu deposition needs to be carefully considered and integrated into a production worthy process to prevent Cu corrosion

Our Metal 1 is in direct contact to source/drain electrodes, which had a Ni/Ge/Au N-type Ohmic scheme. The first two attempts at developing a suitable metal structure resulted in high On Resistance (R_{on}) and low Idss. The problem was caused by high resistance at the Ohmic / Metal 1 interface. Changing the pre-clean process and metal structure resolved the high R_{on} issue. Other than low resistance, the barrier has to fulfill its primary role of blocking Cu atoms from migrating into the semiconductor and the Au atoms in the Ohmic metal into the Cu layer.

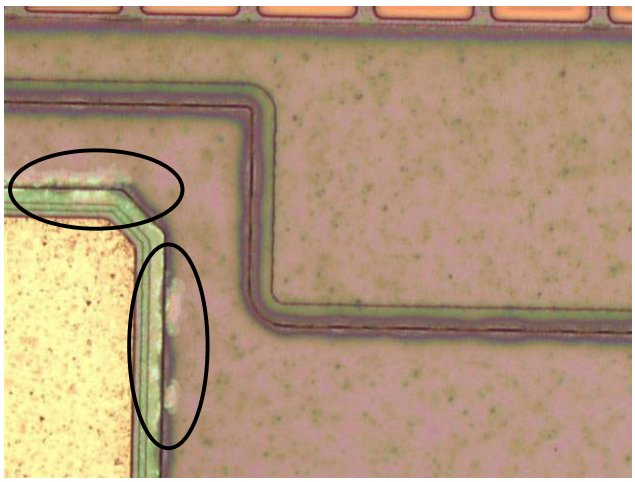

Figure 1 Exposed Cu attacked in pre-clean solution.

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RESULTS AND DISCUSSION

PCM data

A comparison of the PCM (Process Control Monitor) data between the control wafers and the wafers with Cu Metal 1 is summarized in table 1. All DC PCM parameters are very similar with some parameters virtually identical between the two groups of wafer.

The PCM structures for R_{on} and Idss have Metal 1 deposited on ohmic metal. Any degradation in the ohmic / Metal 1 interface, including Cu migration into the ohmic metal, will result in a high resistivity path adversely affecting Ron and Idss. R_{on} for the Cu M1 wafers was 4.125 Ω, which was 3 mΩ higher than control. The small difference is statistically insignificant and is within the tolerance of the test equipment. The R_{on} data correlated with Idss values of 131.0mA and 131.1mA for the control and Cu Metal 1 wafer respectively.

The pinch off voltage (V_p) was slightly higher for the Cu Metal 1 wafers in this experiment. However the difference of 7mV is very small and falls within the normal distribution of Vp.

Gate leakage (Ig) of the Cu Metal 1 wafers was slightly higher than control at 0.229 μA and 0.219 μA respectively. The small difference in Ig can not be attributed to the Metal

1 as the Cu Metal 1 structure did not contact the gate metal. The gate leakage current as well as breakdown voltage are considered good and fall in the normal distribution of the parameter of this mask.

Table 1 PCM data comparison

	Control	Cu Metal1
Ron (Ω)	4.122	4.125
Idss (mA)	131.0	131.1
Ig (μA)	0.219	0.229
Vp (V)	0.935	0.942
Vbr (V)	10.12	10.04
Gm (mS)	167.7	165.5

On Wafer Data

After the PCM test, all wafers received the final silicon nitride passivation. The entire Cu Metal 1 stack has to be able to withstand the process temperature of 300ºC. The barrier can not fail or Cu will migrate into the ohmic metal which will lead to the eventual failure of the device.

Insertion Loss (IL) and 3rd Harmonics were analyzed. As with the DC PCM data, there was little difference between wafers with Cu interconnects and the control.

Both high band and low band insertion loss were normal and the difference between the two groups was less than 0.7%. Based on the results, one can conclude that both DC and RF performance of the Cu M1 wafers was identical to the standard Au metallization and there was no Cu diffusion into the semiconductor under our normal process condition.

Table 2 Circuit data

	Control	Cu Metal1
3rd Harmonic	-61.25 dBm	-61.43 dBm
IL (dB) low band	-0.463	-0.464
IL (dB) high band	-0.430	-0.427

RELIABILITY

The main concern of using Cu in the Metal 1 as the primary conductive layer is Cu diffusion into the semiconductor. As a preliminary reliability test, two PCM tested wafers with the Cu metallization were put through a 48 hour bake, unbiased, at 250ºC. After the bake cycle, visual inspection revealed no discoloration in the metallized area – an indication that no significant amount of Cu had diffused into the Au layer.

Early experiments with standard clean process did result in such defects at a site where exposed Cu was etched. Subsequent attempts with changes in the deposition and clean processes completely eliminated these defects.

Another issue that can arise from a bake is nitride delamination. Small pockets of exposed Cu especially where the Cu interconnects go over a step, is more susceptible to getting etched in wet chemistries. After nitride deposition, a prolonged bake would reveal such sites as the trapped chemicals expand and cause localized nitride delamination. None of the Cu Metal 1 wafers displayed any signs of nitride delamination.

The wafers were retested and the results compared against the pre-bake data. All DC and RF PCM parameters still measured within 5% of the original values.

STEM/EDX analysis

A semi-quantitative analysis was performed, utilizing FIB/STEM to section the source/drain finger. EDX was used to survey several sites in the ohmic metal and in the InGaAs channel. See Fig [2]. No Cu signal was detected in any of the sites surveyed. The small Cu peaks at site 4 were from the sample holder fixtures and grid which were made from Cu.

EDX was also performed on the Cu layer but no Au signal was present.

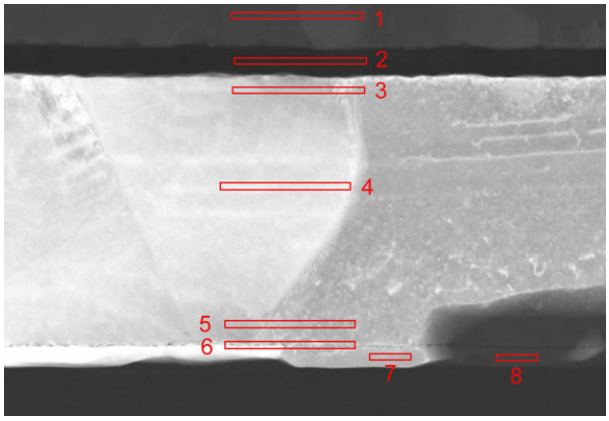

Figure 2 STEM image of Cu Metal 1 on Ohmic

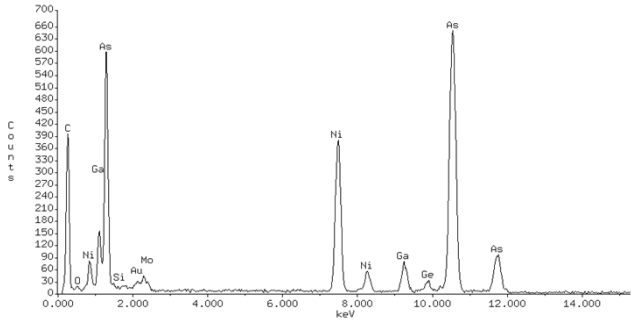

Figure 3 EDX survey of Site 8.

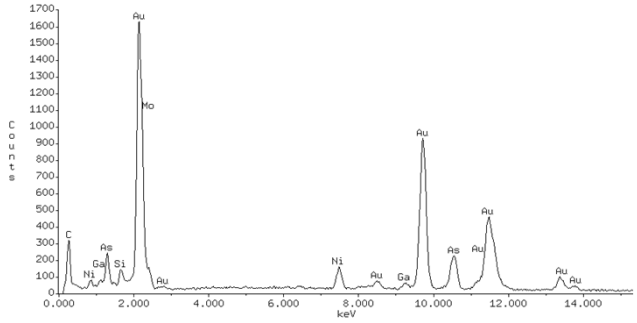

Figure 4 EDX survey of Site 6.

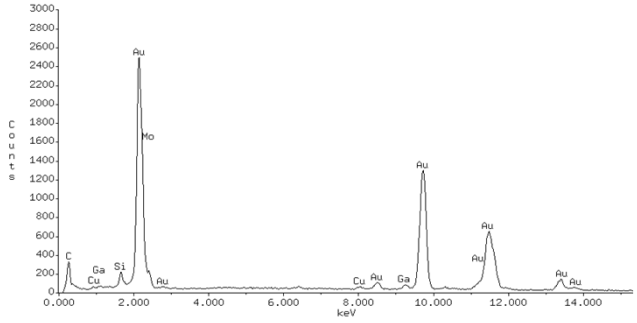

Figure 5 EDX survey of Site 4. Small Cu signal is from the grid.

CONCLUSION

We have demonstrated that Cu is a practical alternative to Au in forming interconnects in a GaAs pHEMT. Our experiments have shown there was no significant difference in DC and RF parameters between the wafers that had Cu interconnects and control wafers. The Cu Metal 1 structure was robust enough to prevent Cu migration after a 48 hour bake at 250ºC with no sign of Cu diffusion into the ohmic metal or other defects. Using E-beam evaporation process to deposit Cu is a simple and cost effective approach. Other than having comparable throughput to electro-plating, E-beam evaporation offers a simplified process by eliminating the seed layer deposition and removal steps from the flow. Our experimental lots yielded well and the wafer passed HTOL reliability test.

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REFERENCES

[1] D. Seghier, H.P. Gislason Effects of Cu on electrical properties of GaAs Semiconducting and Insulating Materials Conference 1998.
[2] B.H. Yang, D. Seghier, H.P. Gislason, Semiconducting and Insulating Materials Conference 1996.
[3] C.Y. Chen, L. Chang, E.Y. Chang, S.H. Chen, D.F. Chang 'Thermal stability of Cu/Ta/GaAs multilayers', Appl. Phys. Lett, vol 77, no.21, 2000.
[4] C.Y. Chen, E.Y. Chang, L. Chang, S.H. Chen 'Backside copper metallization of GaAs MESFETs', Electronics Lett, vol. 36, no. 15, 2000.
[5] K. Holloway, P.M. Fryer Tantalum as a diffusion barrier between copper and silicon. Appl. Phys. Lett, vol.57, no.17 1990.
[6] K. Holloway, P.M. Fryer, C. Cabral, J.M.E. Harper, P.J. Bailey, K.H. Kelleher Tantalum as a diffusion barrier between copper and silicon: failure mechanism and effect of nitrogen additions. J. Appl. Phys., vol 71, no. 11 1992.

ACRONYMS

pHEMT: Pseudomorphic High Electron Mobility Transistor
NMP: N-Methyl Pyrrolidone
HTOL: High Temperature Operating Life
CMP: Chemical Mechanical Polishing
PCM: Process Control Monitor