Improvement in Yield and Assurance in Power Performance for Quarter-Micron Optical Gate 8V Power pHEMT Technology

Cheng-Guan Yuan, S.M. Joseph Liu, Clement Huang, Jiro Ho, Frank Chen, Chien-Liang Chan, Jung-Tao Chung

WIN Semiconductors Corp. No. 69 Technology 7th Rd, Hwaya Technology Park, Kuei Shan Hsiang, Tao Yuan Shien, Taiwan (333).
Website: www.winfoundry.com

Abstract

A low cost and production worthy, 0.25 μm optical gate 8V power pseudomorphic high electron mobility transistor (pHEMT) technology using i-line stepper is developed. With increased photo resist thickness, yield exceeding 95% is demonstrated for devices with 12.5mm gate width across a 6-inch GaAs wafer. In addition, no drain current degradation under the breakdown stress over time test is observed. We find that the Al content of the AlGaAs Schottky plays an important role in current drop phenomenon. Psat of 21.7dBm with PAE of 53.0% and linear gain of 15.6dB is achieved at 10GHz with VDS=8V.

I. Introduction

Traditionally 0.25 μm gate has been achieved using e-beam direct write. But, E-beam direct write tool has limited throughput. Hence in recent years, 0.25 μm gate and sub 0.25 μm gate has been realized using i-line stepper with dielectric assist approach or using DUV stepper [1, 2, 3]. But, these approaches can still be very expensive for high volume manufacturing. Therefore, the alternative of i-line stepper based photolithography is very attractive to GaAs-based electronics when looking into methods of reducing manufacturing costs or improving the throughput. As a leading GaAs wafer foundry, WIN has developed the state-of-the-art i-line stepper technique to realize 0.25 μm gates [4], and 0.15 μm gates [5]. The i-line stepper approach, together with an advanced photo resist reflow process, is potentially the lowest cost solution for next generation applications. The WIN quarter-micron process provides the possibility for low cost production of a high performance X-band T/R chipset [6].

In this paper, we show very high gate yield through optimizing photo resist, and a variant of our quarter-micron optical gate pHEMT technology for power endurance under 8V operation is reported.

II. Device Fabrication

The AlGaAs/lnGaAs pHEMT devices utilize molecular beam epitaxy grown material on 6-inch GaAs substrate. The epi structure consists of a thin, undoped InGaAs channel layer, and double delta-doped layers that provide carriers to the channel. An AlGaAs Schottky layer is placed on top of the upper spacer layer. The Ohmic contact is deposited first and uses the standard AuGeNi type approach. After that, Mesa implantation and selective first recess etch are used to fabricate the MMICs.

The 0.25 μm gate is defined by constructing sequentially with two different resist materials. As sketched in Figure 1, the first resist is coated directly over GaAs substrate. The i-line stepper then exposes this resist at a certain dimension. This resist is then developed and reflowed thermally to have the trench uniformly shrunk down into a 0.25μm opening as required. The second resist is then applied to define the overhang of the T-shape. The gate recess profile is controlled by wet-etch process. The gate level is completed by Ti/Pt/Au evaporation. Thus, this “T” gate metal technology can ensure a low gate resistance.

After the gate definition, the device was fully passivated by SiN. The MIM capacitor designs of both 400 and 600 pF/mm2 are available.

III. Improvement in Yield and Performance

- Gate Yield Improvement

  The excellent yield and reproducibility are mainly related to well controled gate photolithography process. As shown in Figure 2, the original spacing between metals is too small for the liftoff solvents to dissolve the resist.

  By increasing photo resist thickness of the top photo resist, which defines the overhang of the T-shape gate, the photo resist side-wall profile becomes more vertical and shows increased level of undercut. Figure 3 shows the increased photoresist thickness creating a discontinuity or break in the deposited metal pattern allowing for the solvent to easily penetrate and cleanly lift-off the resist and the metal. We could therefore
obtain very high yield of devices with long gate periphery.

Gate yield of each wafer is evaluated using 1x75 μm, 1x250 μm, 24x75 μm, and 50x250 μm devices. Our spec is 0.05mA/mm in drain current defined at grounded source, –2V gate bias and 1.5V drain bias. Figure 4 demonstrates 98.4% of 188 instances of 50x250 μm devices across 6-inch GaAs wafer showing normal FET characteristics with satisfactory drain current pinch off.

Table 1 lists the gate yield of these devices on each of the 18 engineering wafers. Each data point represents the average pinch-off yield of 188 such devices across one wafer. These results show that this 0.25μm optical gate process is repeatable and robust.

- Power Endurance at 8V VDS

A set of control wafers and engineering wafers have been processed and compared. The engineering wafers are varied in their AlGaAs Schottky barrier layer design. We increased the aluminum mole fraction at the Schottky interface.

For operation at VD=7V, control wafers show good power performance, as shown in Figure 5. The maximum gate leakage current is 53μA/mm. But, the gate leakage at 8V operation is around 245μA/mm, which is much higher than that at 7V, as shown in Figure 6. Figure 7 shows that the control 8x75μm device is stable after stressed at 3dB gain compression output power, 3.5GHz, and 7V Vds for 120hours.

To assess its reliability, the breakdown stress over time measurement has been performed. Both the gate-source and drain-source voltage have been applied to the transistor. The transistor is placed under breakdown condition for a duration of time. After the duration of 15 minutes, and after 20 hours, the IV curve is measured. After biased at VG=-3V and VD=12V for 24 hours, a control 2x75μm device shows negligible Id reduction, as shown in Figure 8. But, as VD bias is increased to 14.5V, Ig increases and the amount of Id reduction increases, as shown on Figure 9. Decrease in Idmax can lead to pre-mature output power reduction of the amplifier. While it is concluded that 7V operation is stable, this work seeks to improve the breakdown characteristic and provide 8V Vds operation.

The degradation mechanism of maximum drain current in AlGaAs/InGaAs pHEMT transistors is caused by an increase in drain resistance [7]. It originates from a degradation layer, possibly containing a significant amount of certain oxide formed at the drain recess surface region. This layer decreases Idmax.

In this study, we successfully stabilize the Id in the engineering wafers. As sketched in Fig. 10, the Schottky barrier layer of the new epi structure has a high Al-content of a certain amount of AlGaAs layer at the Schottky interface. With the insertion of this layer, we have achieved negligible Id reduction after the breakdown stress test. After 20-hour stress, all samples show no current reduction, as shown in Figure 11. Figure 12 demonstrates the loadpull measurements of a 2x75μm device taken at 10GHz with VDS=8V, 153mA/mm IDS. Psat of 21.7dBm (992mW/mm) with maximum PAE of 53.0% and linear gain of 15.6dB is provided.

IV. Summary

A cost-effective and excellent yield of a quarter-micron optical gate power pHEMT MMIC process is presented in this paper. The simplicity of the optical gate process makes this technology suitable for high-yield production. Power endurance can be achieved by using high Al-content on the Schottky interface. This allows 8V operation for power amplifier application.
Figure 3. The increased photoresist thickness creates a discontinuity or break in the deposited metal pattern allowing for the solvent to easily penetrate and cleanly lift-off the resist and the metal.

Figure 4. 98.4% of 188 instances of 50x250 µm devices across 6-inch GaAs wafer show normal FET characteristics with satisfactory drain current pinch off. Our spec is 0.05mA/mm in drain current defined at grounded source, –2V gate and 1.5V drain bias. (Unit: mA/mm)

Table 1. Each data point represents the average yield of 188 instances of each device across 6-inch GaAs wafer. These results show that this 0.25µm optical gate process is repeatable and robust.

Figure 5. The P3dB gate leakage current of a 2x75µm device at 7V operation is 8uA (53uA/mm).

Figure 6. At 8V, the P3dB gate leakage current of a 2x75µm device is 36.7uA (245uA/mm).

Figure 7. The 8x75µm device is stable after stressed at 3dB gain compression output power, 7V Vds.

Figure 8. After biased at VG=-3V and VD=12V for 24 hours, this device shows negligible Id reduction.
Figure 9. This 2x 75μm device is stressed at VS=0V, VG=-3V and VD=14.5V. After 20hr stress, the current of this device shows ~37.7% degradation.

Figure 10. The high Al content of a certain amount of AlxGaAs layer on Schottky surface can suppress Id reduction of the breakdown stress test.

Figure 11. After 20hrs stress at VS=0V, VG=-3V and VD=14.5V, this 2x 75μm device shows no current density drop.

Figure 12. A Psat power of 21.7dBm with maximum PAE of 53.0% is achieved at 10GHz, 8V VDS. The P1dB is around 20.5dBm (750mW/mm).

References


