A Foundry-Ready Ultra High $f_T$ InP/InGaAs DHBT Technology

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Abstract

An ultra-high-$f_T$ InP/InGaAs DHBT technology has been developed and qualified for foundry service. The device has $f_T$ of up to 300GHz, $f_{max} > 250$GHz, and is very reliable, with MTTF >2x10^6 hours at $T_J$ of 125°C. This technology is an ideal candidate for high-speed digital, millimeter-wave and mixed-signal circuits. Tradeoffs between $f_T$ and BVCEO have been studied and advantages of InP DHBT over InP SHBT and SiGe HBT are reported in this paper.

INTRODUCTION

InP/InGaAs HBT is an excellent electronic device for optical communication systems and high-frequency test instruments due to its high speed and low power consumption. InP HBTs with $f_T > 150$GHz have been used as foundry process to manufacture high-speed products at GCS for several years [1]. Although they can meet current 40 to 50Gbps applications, there are demands for higher speed and higher bit rate applications such as cloud computing, which require ultra high $f_T$ devices, and some millimeter-wave circuits that require decent breakdown voltage and good threshold voltage control. InP based HBTs are good candidates for these applications. There are several reports of InP/InGaAs [2] and InP/GaAsSb [3] HBTs with $f_T > 300$GHz, but they typically require operating current density of >500kA/cm² in order to achieve the reported high $f_T$. This high current density would raise the device junction temperature to such a high level that could cause reliability concerns. InP DHBT for 100Gbps application has been demonstrated, but no reliability data were reported [4]. Moreover, these advanced InP HBT processes are not available for open foundry services. In this paper, we report ultra-high-$f_T$ InP/InGaAs DHBTs with $f_T$ of up to 300GHz and MTTF >2x10^6 hours at $T_J$ of 125°C. This technology is readily available for foundry services with a reliability report and a complete design kit.

DEVICE FABRICATION

The ultra-high-$f_T$ InP DHBT epi structures consist of an InP emitter, a thin carbon-doped InGaAs base, and an InP collector structure with a grading layer between InGaAs base and InP collector to eliminate electron blocking. Two DHBT structures (DHBT2 with $f_T$ of 250GHz and DHBT3 with $f_T$ of 300GHz) with different collector thickness were designed and fabricated. The key process steps include self-aligned emitter/emitter mesa, non-self-aligned base metal, base mesa, collector metal, and collector mesa. Metal posts on base and collector metals are used to make their heights at the same level as that of emitter metal. BCB is used for device passivation and planarization. BCB etch-back process is employed to expose emitter, base and collector posts for the first-level metal to access those three contacts. BCB is also used as low-loss interlayer dielectric between first and second level metals. TaN TFR and Si₃N₄ MIM capacitor are used for monolithic integration of passive components. Backside through-substrate via with low-inductance grounding is available to further enhance the circuit performance and design flexibility. All InP HBT processes are on 4-inch wafers. Standard HBT emitter sizes are 0.8x3μm², 0.8x6μm², and 0.8x10 μm². Fig. 1 shows the SEM pictures of a 0.8x3μm² DHBT (a) prior to BCB passivation and (b) posts and first-level interconnect metal.

DEVICE PERFORMANCE

Figure 2. Typical IV curves of a 0.8x5μm² DHBT3 device. Solid lines are measured data and dots are modeled data.
Fig. 2 shows the typical IV curves of a 0.8x5 μm² DHBT3 device. The Vce offset voltage is 0.15V, and the knee voltage is 0.5V at Jc = 300kA/cm², which are similar to those of an SHBT, indicating that there is no electron blocking effect in the base-collector heterojunction. The typical current gain is ~40 at Jc of 100 kA/cm² for both DHBT2 and DHBT3. Fig. 3 shows a typical wafer map of the current gain distribution for a 0.8x3 μm² DHBT3 at Jc = 100kA/cm² on a 4-inch wafer.

On-wafer small-signal RF performance was measured with vector network analyzer from 0.5 to 40GHz. Fig. 4 shows the measured |H21| and maximum stable/available gain, MSG/Gmax, as functions of frequency. fT and fmax are extrapolated by using a −20dB/decade slope. Due to frequency limitation of our test equipment, the onset of maximum available gain is beyond 40GHz and the extrapolated fmax value of 250GHz at Jc = 300kA/cm² may be underestimated. Fig. 5 shows fT vs. Jc at Vce=1.0V, 1.5V, and 2.0V of a DHBT3 device. fT reaches 290GHz and 300GHz at Vce=1.0V, Jc =300 and 400kA/cm², respectively.

To provide optimum performance for different applications, tradeoffs between fT and BVceo have been studied. Both SHBTs and DHBTs with different collector structures were designed and fabricated for comparison. Fig. 6 shows fT vs BVceo for InP DHBTs and InP SHBTs with different collector thickness designs. A SiGe HBT data [5] is also included as reference. Although BVceo is affected by current gain and collector doping, it is mainly determined by the collector thickness and band-gap. If we use fT•BVceo as the figure of merit (FOM), it is clearly shown that DHBT offers the best FOM. Since the InP DHBTs of this work are aimed for high-speed digital, millimeter-wave, and mixed-signal applications, BVceo of >3.5V can meet the requirement for most of the applications. In comparison, BVceo of InP SHBT is about 1.7V lower than that of DHBT with the same fT. Therefore, DHBTs have been chosen for foundry services to provide a higher breakdown voltage while maintaining ultra high fT.
Table 1. Summary of typical DC and RF data for GCS' InP HBT devices. SHBT and DHBT1 are first-generation foundry devices. DHBT2 and DHBT3 are advanced high $f_T$ devices.

<table>
<thead>
<tr>
<th>HBT Parameters</th>
<th>Unit</th>
<th>SHBT</th>
<th>DHBT1</th>
<th>DHBT2</th>
<th>DHBT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Size</td>
<td>µm²</td>
<td>1x3</td>
<td>1x3</td>
<td>0.8x3*</td>
<td></td>
</tr>
<tr>
<td>Beta at $J_c=100kA/cm^2$</td>
<td></td>
<td>35</td>
<td>35</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Typical operating current density, $J_{ct}$</td>
<td>kA/cm²</td>
<td>100</td>
<td>100</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Maximum operating current density, $J_{cm}$</td>
<td>kA/cm²</td>
<td>200</td>
<td>200</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Typical operating voltage, $V_{cc}$</td>
<td>V</td>
<td>1.0</td>
<td>2.5</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>Base-collector breakdown voltage, $BV_{cbo}$</td>
<td>V</td>
<td>4.0</td>
<td>4.0</td>
<td>5.5</td>
<td>4.5</td>
</tr>
<tr>
<td>Collector-emitter breakdown voltage, $BV_{ceo}$</td>
<td>V</td>
<td>3.5</td>
<td>7.0</td>
<td>4.5</td>
<td>3.8</td>
</tr>
<tr>
<td>$V_{cc}$ offset voltage, $V_{cc}$</td>
<td>V</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
</tr>
<tr>
<td>$f_T$ (at Max allowed operating current)</td>
<td>GHz</td>
<td>200</td>
<td>150</td>
<td>250</td>
<td>290</td>
</tr>
<tr>
<td>$f_{max}$ (at Max allowed operating current)</td>
<td>GHz</td>
<td>200</td>
<td>150</td>
<td>240</td>
<td>250</td>
</tr>
<tr>
<td>Thermal resistance, $R_{th}$</td>
<td>°C/mW</td>
<td>9.9</td>
<td>5.3</td>
<td>5.3</td>
<td>5.3</td>
</tr>
</tbody>
</table>

*: 0.8x5 and 0.8x10 µm² devices have the same DC (scaled) and RF performance as those of 0.8x3 µm² devices except for $R_{th}$.

Table 1 summarizes the DC and RF performance of all GCS InP HBT devices. SHBT and DHBT1 are first-generation devices for 40-50Gbps applications as described in a previous publication [1]. DHBT2 and DHBT3 are new technologies with ultra high $f_T$. The advantages of a DHBT structure are not only to achieve higher $f_T$ and higher $BV_{ceo}$ simultaneously but also to provide lower thermal resistance as compared to that of SHBT. In comparison with SiGe HBT technology, the performance parameters of InP DHBTs shown here are much better than those of SiGe HBTs. For example, a 300GHz-$f_T$ SiGe HBT has a $BV_{ceo}$ of only 1.85V and it requires much smaller emitter size and 10 times higher current density than its InP DHBT counterpart reported in this work in order to achieve the same 300GHz $f_T$ [5].

**DEVICE MODELING**

We have modeled all three different-size devices for both DHBT2 and DHBT3 using measurement data at different bias conditions ($V_{cc}$ from 1.0V to 2.0V and $J_c$ from 30kA/cm² to 300kA/cm²) and at three temperatures, (25, 50 and 75°C). ADS design kits have been developed for this technology. An example of good fitting between modeled and measured data is shown in Fig. 3 for DC IV curves. Fig. 7 shows good fitting of s-parameter for a 0.8x5 µm² DHBT3 device at $J_c$ of 200kA/cm² and $V_{cc}$ of 1.5V in the frequency range of 0.5 to 40GHz.

**RELIABILITY**

We have also completed qualifications of DHBT2 and DHBT3 devices by high temperature stress test. HTOL test was performed at two different junction temperatures, 248 and 269°C, at $J_c$ =300kA/cm². Four groups with ten 0.8x3µm² devices in each group were tested. Fig. 8 shows the normalized beta versus high-temperature stress time at $V_{cc}$=1.25V, $J_c$=300kA/cm² and $T_j$=248°C for 10 DHBT3 devices. With the device failure criterion defined as 20% beta degradation at $J_c$=100kA/cm², the MTTF for this group was 1028 hours. There were no infant failures in all groups tested. The typical device failure mode was base current increase. Fig. 9 shows the Gummel plots of a failed device before and after 1661 hours of high-temperature and high-current stress. The base current increased significantly in the low voltage region, mainly due to base surface recombination current increase, which is the typical HBT failure mechanism. Fig. 10 shows the Arrhenius plots for both DHBT2 and DHBT3 devices at two temperatures. The extrapolated MTTF is >2x10⁶ hours at $T_j$=125°C, and the activation energy (Ea) is >1.1eV, which could meet most application requirements. To the best of our knowledge, most InP HBT reliability data reported in the literature have been tested at $J_c$ of about 100kA/cm² [6]. The reliability data of this work show that DHBT2 and DHBT3 have excellent reliability at $J_c$ of 300kA/cm².
In summary, we have developed and qualified an ultra-high-\(f_T\) InP/InGaAs DHBT technology for foundry service. Relationship between \(f_T\) and \(BV_{CEO}\) has been studied with different collector designs. Two DHBT devices with \(f_T-BV_{CEO}\) trade-offs are available in this technology. \(f_T\) of up to 300GHz and \(f_{MAX}>250\)GHz for DHBT3 device with \(BV_{CEO}\) of 3.5V have been achieved. DHBT2, which has \(BV_{CEO}\) of 4.5V and \(f_T\) of 250GHz, is a good candidate for applications that require higher breakdown voltage. ADS design kits have been developed for this technology. Both DHBT2 and DHBT3 devices are very reliable with MTTF >2x10^6 hours at \(T_J\) of 125°C. This InP/InGaAs DHBT technology is an ideal candidate for 100Gbps electronic circuits such as TIA, and for high-speed digital, millimeter-wave, and mixed-signal circuits.

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**REFERENCES**


**ACRONYMS**

HBT: Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
SHBT: Single Heterojunction Bipolar Transistor
\(f_T\): Cutoff frequency
\(f_{MAX}\): Maximum oscillation frequency
\(J_C\): Collector current density
\(H21\): Small signal current gain
MIM: Metal-Insulator-Metal
TFR: Thin Film Resistor
HTOL: High Temperature Operating Life
\(T_J\): Junction temperature
MTTF: Median Time To Failure.
\(E_a\): Activation energy
TIA: Transfer-Impedance Amplifier