The Development of 0.5-μm High Linearity and Good Thermal Stability AlGaAs/GaAs HFET for Wireless Infrastructure

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Keywords: GaAs, HFET, Linearity and Thermal Stability

Abstract

Heterostructure FETs (Doped-Channel FETs) have been widely used for high linearity requirement system such as digital wireless communication infrastructure due to its excellent electron confinement ability and superior Schottky barrier height characteristics.

In this paper, we report the development status of the 0.5-μm gate-length double-recess GaAs HFET. A 1.2-mm device can achieve P1dB output power of 21.5 dBm with a third order intercept (TOI) point of 43 dBm, where device was biased at Vds=5V and 50% of Idss operation at 0.5 GHz frequency operation. In this technology, it is critically important to develop a high thermally reliable device. After optimization transistor layout configuration such as and gate-to-gate pitch and specific wide-recess etching process, there is no obviously current degradation was observed on 4.8-mm devices, which are operated at Vds=8V and 50% of Idss operation under 75 C ambient-temperature for 168 hours.

INTRODUCTION

The AlGaAs/GaAs Heterostructure FETs (Doped-Channel FETs) have been widely used for high linearity requirement system such as digital wireless communication infrastructure due to its excellent electron confinement ability without any real space transfer. Moreover, the AlGaAs insulator can improve the breakdown voltage resulting in an increase of maximum output power [1]. Currently, there are several foundry companies have provided this technology for this market application. [2]-[3].

From customer's perspective, WIN semiconductors corporation should develop a good electrical performance with high robust HFET technology as same as our competitors. Hence, we started to develop this technology since February 2006, and officially released this technology on December 2009.

In this paper, we report the technology development status, which includes the design of epitaxial structure and the critical gate process. Moreover, after evaluating the device-level dc, small-signal and power performance, we reveal the current degradation on 4.8-mm devices after DC-HTOL for 168 hours by using our preliminary process and unit-cell design.

The device performance degradation is caused by high junction temperature operation and hot-election effect [4]. Therefore, we demonstrate the sequence of the device process optimization such as increasing gate-to-gate spacing, wide-recess spacing optimization, field-plate process, and specific wide-recess process to reduce the junction temperature and minimize the impact of the hot-electron effect.

EPITAXIAL STRUCTURE DESIGN AND CRITICAL GATE PROCESS

Fig. 1 shows the cross-section of HFET epitaxial structure, which is grown by the MBE on 150-mm semi-insulating GaAs substrate. The epitaxial structure was designed to be compatible with double selective gate recess etch process using AlGaAs and GaAs as the Schottky insulator layer and channel layer, respectively. The layer thickness, channel and doping concentration was designed to obtain the optimum trade-off among parameters, such as breakdown voltage, pinch-off voltage, and transconductance.

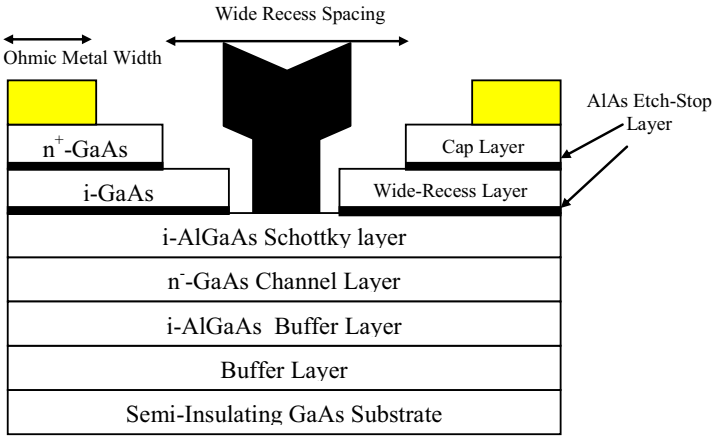


Fig. 1 The schematic epitaxial structure cross-section of the HFET technology.

Fig. 2 shows the SEM cross-section of 0.5-µm T-shape gate which was done by using bi-layer process. The advantage of this process is that the small recess undercut can be obtained, which means that the surface effect near by gate metal will be minimized.

Regarding the passive components, we provide 2 metal interconnect layers with low-k polymide di-electric layer, 50 ohm/square TaN resistors, 250 ohm/square epi-resistors, 600 pF/mm2 MIM capacitors. And, the final protect nitride will be adopted for reliability concern. Finally, the substrate will be thinned down to 4-mil thickness with 4-um plating gold backside via process.

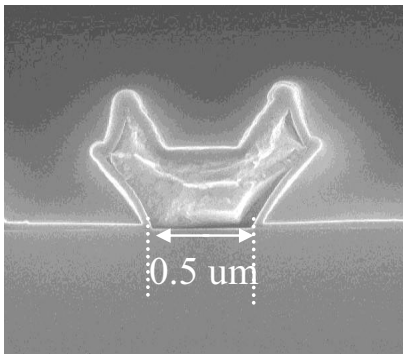


Fig. 2 SEM Cross-section of the T-shape Gate in HFET Technology

DEVICE DC/RF CHARACTERISTICS

The HFET dc transfer characteristics are shown in Fig. 3, which exhibits flat transconductance characteristics. The threshold voltage (I_{ds}=1mA/mm) and the I_{dss} are –2 V and 240 mA/mm respectively. On-wafer microwave S-parameter evaluation was carried out by using network analyzer. Table 1 summarizes the relative characteristics of AlGaAs/GaAs HFET..

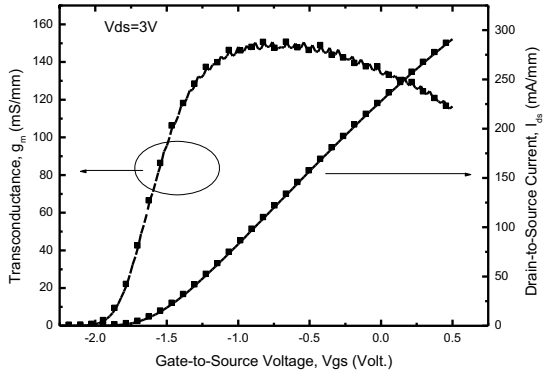


Fig. 3 DC Ids-gm-Vgs characteristic of the AlGaAS/GaAs HFETs for 0.5-µm T-gate-length devices.

Table 1 Summary of DC and RF characteristics of AlGaAS/GaAs HFET's.

AlGaAs/GaAs HFET					
V_{to} (volt.)	I_{dss} (mA/mm)	V_{dg} (Volt.)	g_m (mS/mm)	f_t (GHz)	f_{max} (GHz)
-2.0	240	>20	145	20	55

As to the rf-power performance, table 2 shows summary of the 0.5-um AlGaAs/GaAs HFET linearity characteristics, which are all carried out by WIN's customers. The frequency range is from 0.5GHz to 3.5 GHz. A 1.2-mm device can achieve P1dB output power of 21.5 dBm with a third order intercept (TOI) point of 43 dBm, where device was biased at Vds=5V and 50% of Idss operation at 0.5 GHz frequency operation.

Table 2 Summary of Linearity characteristics of AlGaAS/GaAs HFET's.

Device Size	HFET 8x150 um
Vdd	5V, Ta=25 C
Quiescent drain current	80 mA/mm~130mA/mm
Gain	10~15 dB
OIP3	40~45 dBm
P1dB with IP3 load	20~21.5 dBm
Noise Figure	1.2~3 dB

Basically, customers were satisfied the device's dc and rf power performance for their product application. However some of customers found that after high power load-pull test, the devices current dropped about 10% for the same Vgs and did not recover. Moreover, customer also pointed out that the 6~7 dB IMD3 degradation on 4.8-mm devices also can be seen after two-tone P1dB over-drive test for 23 hours under ambient temperature is 60 C.

According to WIN's internal reliability test requirement, any new technology needs to pass the DCHTOL test under junction temperature is 125 C for three lots. However, the device size is only 2x75-um, and we didn't see any current degradation on small devices.

In order to investigate the current and linearity degradation effect we have built up two systems for measuring DC and RFHTOL on large-periphery devices. Fortunately, we also observed the 10% current degradation on 4.8-mm devices, which bias at Vds=8 V, and Ids ~600 mA under 75 C ambient temperature for 168 hours as shown in Fig. 4.

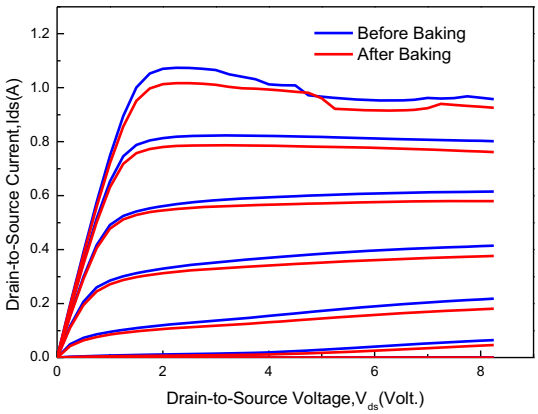


Fig. 4 The DC-IV characteristics of a 4.8-mm device before and after electrical stress under 75 C ambient temperature for 168 hrs.

HOW TO IMPROVE DEVICE'S CURRENT DEGRADATION.

First of all, we tried to enlarge the ohmic width of device from 20-µm of preliminary design to 35-µm as shown in Fig. 1, which is equal to increasing gate-to-gate pitch so that the thermal coupling effect can be decreased. Table 3 summaries the results of current degradation on 1.2-mm devices after 168 hours DCHTOL by using various ohmic widths. As we can see, the current degradation effect can be improved from 4.5% to 3 % by adopting 35-µm ohmic width. The drawback of this method is that device size will also be extended. The device size will be increased about 26% and 33% for 1.2-mm and 4.8-mm devices respectively. We further applied the 35-um ohmic width for 4.8-mm devices as well. As we can see in Fig. 7, the current degradation can be improved from 10% to 5.7% on 4.8-mm devices. Nevertheless, the current dropping still can't be fully resolved by using wider ohmic width.

Table 3 Summary of Current Variation of 1.2mm devices after DC-HOTL

Ohmic Width (µm)	Gate-to-Gate Pinch (µm)	**Current Variation
15	16.5	-5.97%
*20	21.5	-4.51%
25	26.5	-4.5%
35	36.5	-3%

*20-um is the Preliminary design, ** Vgs=0 V, Vds=5V.

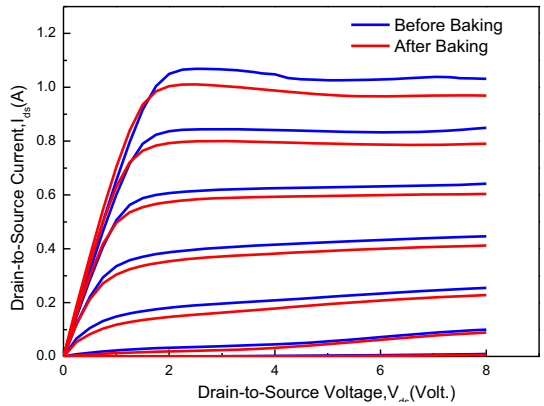


Fig. 6 The DC-IV characteristics of a 4.8-mm device with 35-mm ohmic width before and after electrical stress under 75 C ambient temperature for 168 hrs.

Another mechanism could cause current degradation is hot-electron effect. At high junction temperature condition, hot electrons are generated near the drain end of the channel where the electrical field is the highest. Hot electrons can accumulate sufficient energy to tunnel into the silicon nitride passivation to form permanent traps. Those permanent traps increased the surface depletion and then caused the open-channel drain current degradation [4].

As we mentored in previous section, we adopted the T-shape process for gate-metal formation so that we can get small recess under cut after gate-recess etching, which means the surface effect nearby the gate can be minimized. However, the width of wide-recess region generally is 1.5 to 2.5-µm, where the wider-region provide space for hot-electron to permeate into SiN layer. Furthermore, the originally purpose of wide-recess design is to get 5~6 V extra breakdown voltage as compared with single recess process. Consequently, the low-doping design is often used in this region as same as Schottky layer to get higher breakdown voltage, which means the lower doping design in wide-recess region can be easily depleted by surface effect.

In order to verify this impact of hot electron, the filed-plate was applied and placed on top of wide-recess region, where the electrode of the filed-plate is directly connected to the gate pad. Fig. 5 shows the cross-section of field-plate metal with 0.5-µm T-gate.

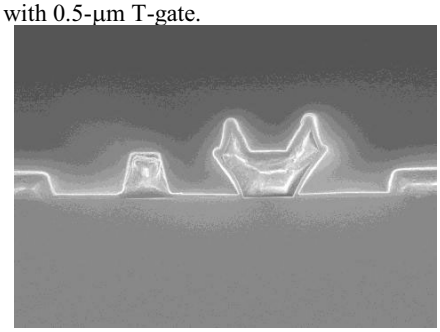


Fig. 5 SEM Cross-section of the filed-plate process in HFET Technology

As we can see in Fig 6, the current degradation can be fully resolved by using filed-plate approach. It is showed that high electron filed generated from filed plate can stop hot electron tunnel into the silicon nitride. However, the rf – characteristics of filed plate device is unacceptable. The ft will be decreased from 15 GHz to 10 GHz at Vds=5 V. On the other hand, the process complexity, process cycle time, and linearity performance degradation will be the drawbacks.

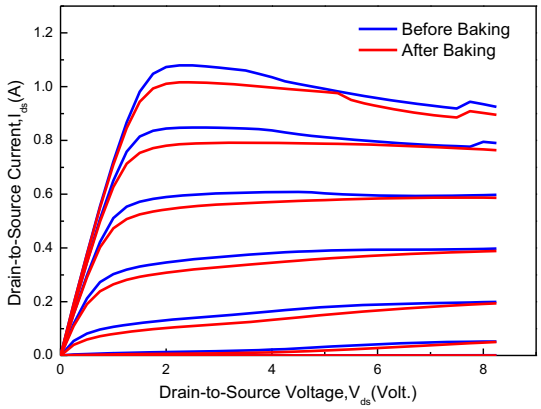
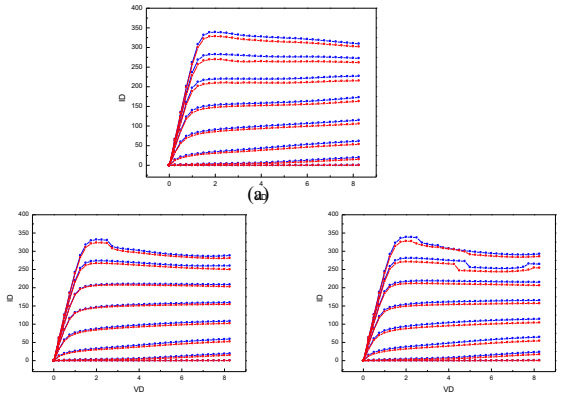


Fig. 6 The DC-IV characteristics of a 4.8-mm device with field-plate before and after electrical stress under 75 C ambient temperature for 168 hrs.

Moreover, the design of wide-recess width also can determine the current stability at high bias region [5].

Total three different wide-recess widths on 1.2-mm devices had been used for the reliability test. The device with smaller wide-recess width such as 1.5-um the can

demonstrate good current stability as shown in Fig. 7(a). Nevertheless, the devices with 1.5-um width recess width can't withstand long-term reliability test. The yield is pretty low especially in 4.8-mm devices. Therefore, the width of wide recess we adopted for this technology is 2-µm and source-to-drain spacing is 3.5-µm



(a) (b) (c)

Fig. 7 The DC-IV characteristics of 1.2-mm devices with wide-recess width of 1.5-um (a), 2-um (b), and 3-um (c), respectively.

Accordingly, the issue is that how to prevent the hot electron penetrate into silicon nitride layer without rf performance decent. As shown in Fig. 2, the two AlAs layers are used for selective etching. Normally, the AlAs layer between cap and wide-recess layer will be removed after cap-layer wet-etching process. If we can keep this layer under the wide-recess layer, the wide bandgap material can be used as barrier layer to prevent or reduce the possibility for the electrons tunnel into the silicon nitride layer.

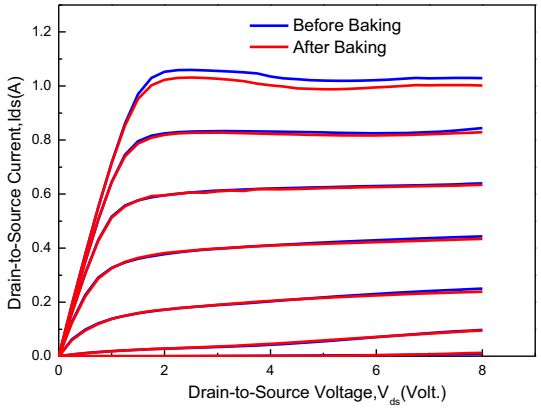


Fig. 8 The DC-IV characteristics of a 4.8-mm device with optimization design before and after electrical stress under 75 C ambient temperature for 168 hrs.

Fig. 8 shows the DCHTOL performance of devices with 35-µm ohmic width, 2-um wide recess width and AlAs layer on top of the wide-recess layer. No current degradation was observed on 4.8-mm devices, which are operated under 75 C ambient-temperature for 168 hours. The junction temperature and thermal resistance of 4.8-mm device are 118 C and 21 (C/W), respectively.

As to the linearity performance as shown in Fig. 9, we also didn't see significant performance different after 5-dB power compress stress at 3.5 GHz fro 90 hours under 75C of ambient temperature.

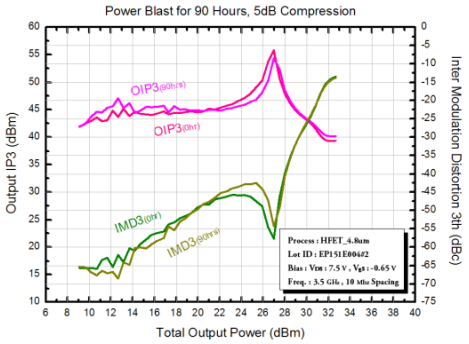


Fig. 9 Two-tone measurement results of 4.8-mm device with optimization process after power stress test for 90hurs.

CONCLUSIONS

In summary, after optimization of device configuration and process, high thermally stable performances with good linearity performance of 0.5-µm AlGaAs/GaAs HFETs have been demonstrated. The results represent this technology offers a great potential for design of high linearity requirement wireless applications.

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ACRONYMS

HFET: Heterojunction Field Effect Transistor