High Volume Test Methodology for HBT Device Ruggedness Characterization

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Abstract

   Developing rugged transistors requires careful consideration of the HBT's collector design. In this work we present a test methodology for high-volume, in-line measurement of device ruggedness. This method is useful not only when developing new epitaxial structures for HBT devices, but also allows in-line monitoring of the device ruggedness for possible deviations due to epitaxial or manufacturing process variations. Moreover, the test is non-destructive.

INTRODUCTION

   InGaP/GaAs and SiGe heterojunction bipolar transistors (HBTs) are widely used for wireless applications since they have excellent features such as high power density and high efficiency. One of the requirements for these technologies, especially for GSM applications or other applications where devices are operated close to saturation conditions, is device ruggedness under high VSWR conditions.

   To increase the device ruggedness many manufacturers develop novel HBT collector designs with proprietary collector doping profiles or super-junction epitaxial structures [1, 2]. Characterization of device ruggedness is an important step in the development of new structures. To date, many of these studies have been based solely on device simulations, with few presenting actual device measurements. One of these earlier works studied the impact ionization induced snap-back in Silicon BJTs by sweeping the device Vce beyond the snap-back locus at various collector current densities. This was accomplished by adding a load resistor in the collector bias line, with a resistance larger than the largest negative resistance of the device in snap-back [3, 4]. Unfortunately, this method has some inaccuracies since the collector voltage at the device was not monitored during the sweep; instead, this voltage is back-calculated based on the measured collector current and the load resistance. In addition, this method is not desirable in a high-volume test environment.

   We present an improved test methodology for high-volume, in-line measurement of device ruggedness based on the above. This new method is useful for both developing new epitaxial structures for our devices and monitoring the device ruggedness in-line to detect deviations due to epitaxial or manufacturing process variations. Moreover, this method is non-destructive.

HARDWARE IMPLEMENTATION

   The current hardware implementation is determined by the device technology and the hardware capabilities. First of all, since we are forcing the devices into bias points beyond breakdown, we need to avoid oscillations. To achieve this we use devices which are laid out with GSG (Ground-Signal-Ground) pads and use RF probes (these are standard structures for RF process control monitors). Testing takes place in screened, fully enclosed wafer probers.

   To overcome the device negative resistance in breakdown, we attach a resistor network directly on the RF collector probe (Figure 1). The resistor network is encapsulated in a metal box. It is extremely important that the path length between the collector and the resistors is kept as short as possible to minimize its capacitance. Standard coaxial cables have stray capacitance of 100 pF/m. The associated capacitance will generate enough charge to destroy the device beyond the snap-back point, during the transient phase of the breakdown.

   The device size is limited by the oscillation suppression condition since smaller devices have much higher impedance, but also by the hardware capability. In order to drive a current density approaching 1 mA/um^2 and at the same time be able to use a force resistance R_f that is large enough to overcome the negative device resistance during snap-back, we determined that the device area should be below 15 um^2. This will ensure that less than 100 V will be needed from SMU2. Moreover, larger devices will be prone to thermal failure during the measurement given the high DC power consumed beyond snap-back.

   In this work, we determined that the best compromise is to use a small device of approximately 5 um^2 emitter area. This device size was proven to work independent of the epitaxial structure used. The force resistor has a value of 8 kOhm, which ensures that the maximum voltage required to deliver 1 mA/um^2 current density is below 70 V, depending on the specific epitaxial structure. For convenience, the sense resistor R_s was chosen to be 16 kOhms. Both resistors are high quality metal film with very low associated

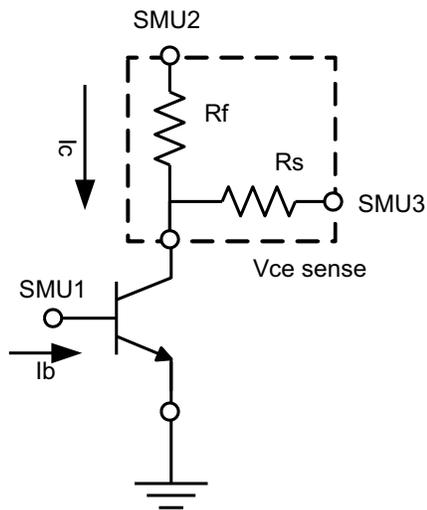capacitance to minimize the charge available to the device during the snap-back event.

Figure 1. Measurement setup.

TEST METHODOLOGY

The devices fabricated for this study consist of a variety of material structures grown by Kopin Corporation and processed in Skyworks Solutions Newbury Park GaAs Fab. The tested HBT is a single emitter of square shape, one base contact and one collector contact. The device is laid out with RF pads.

The main test involves sweeping the collector voltage beyond the device snap-back voltage and monitoring the collector current. However, since the main purpose is to compare and monitor various epitaxial structures or technologies, we first need to determine the necessary base currents needed to achieve the same collector current densities before the snap-back occurs. To accomplish this we measure a Gummel sweep on the device. The sweep is not trivial given the fact that we cannot disconnect the resistor network during the two separate tests. Adding a switch matrix for automated switching of the resistor network is not possible either since the additional cabling will add capacitance to the device collector and result in the device failure during the snap-back event.

To overcome this limitation, the base and collector SMU1 and SMU2 are synchronized. The ICCAP driven test setup which includes an HP 4142B bias unit allows sweeping the current on the base SMU while synchronizing the collector SMU to deliver a voltage with an 8,000xBeta ratio (forcing resistor multiplied by the expected device DC current gain) and a 5V offset. In effect, this test condition coarsely emulates the Gummel sweep. In reality, the device DC gain varies depending on the current. Hence, this test condition is equivalent with a varying collector voltage

Gummel. However, for the current density range of interest in this work between 0.1 mA/um^2 and 0.8 mA/um^2, this test is a good approximation. An initial guess of a DC gain of 115 is a good starting estimate for our devices independent of the epitaxial structure, which insures good results even if the actual gain falls between 90 and 130.

After the initial Gummel test, we calculate the needed base current that will deliver a collector current density in increments of 0.1 mA/um^2 up to the maximum current of interest (Figure 2). The test subsequently sweeps the collector SMU2 voltage from 0V to the maximum voltage needed to achieve the device current density limit of 1 mA/um^2. The SMU3 forces no current and monitors the collector voltage. Since the forcing resistor is larger than the most negative device resistance we are able to monitor the collector voltage beyond the snap-back locus without damaging the device.

SOA ANALYSIS

A typical ruggedness device test is presented in Figure 2. Several device parameters are extracted from these curves. First, BVceo is recorded as the maximum collector voltage while the collector current is still substantially low and the controlled base current has a value needed to generate a 0.001 mA/um^2 device current density. We also record the maximum collector voltage for the same curve, BVce_max, and the associated current density J_BVce_max, and the maximum current achievable during snap-back at BVceo, Jmax.
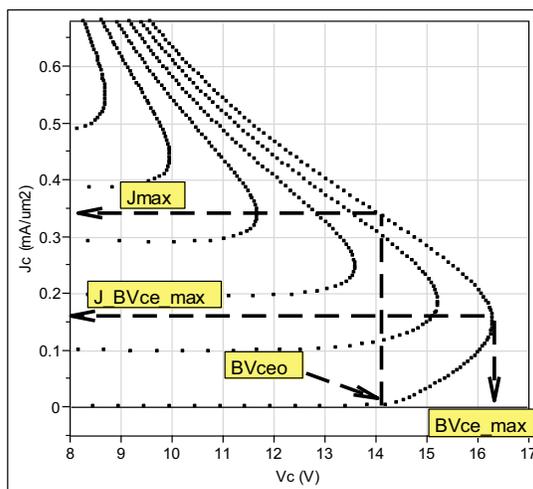

Figure 2. Breakdown parameters are extracted from the Jc-Vce curves.

Furthermore, the test algorithm collects the locus of the Jce-Vce points that define the snap-back. This is the collection of points on each curve where the derivative of

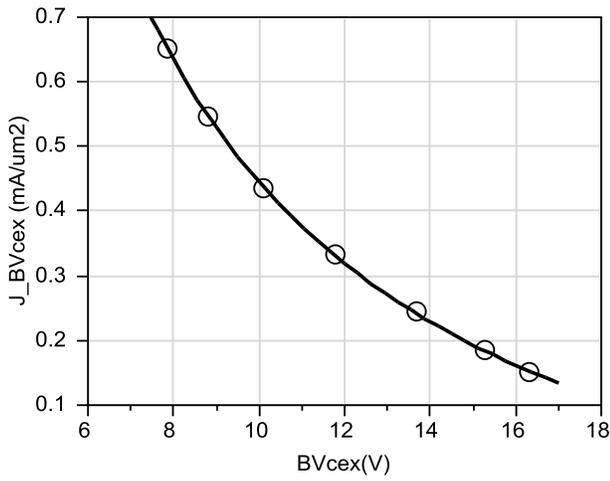Vce with respect to Ic becomes zero. The envelope of the points is referred to as the SOA limit (Figure 3).

Figure 3. Measurement and fit of the snap-back Jc-Vce locus points (circles – measurement, curve – Vce^{-1} linear fit).

Given the fact that we are forcing a constant base current, thus the impedance that the device base sees is very high, this SOA boundary is somewhat limited in scope. Indeed, if the base is ballasted with a base resistor and biased with a voltage source, a different SOA boundary will be defined [2]. Given the test setup in our work, the determined SOA boundary represents the limit of device safe operation when the device is biased using a current source in the base, similar to a GSM power amplifier. Previous research has shown that when the base is biased with a voltage source through a ballast resistor, higher snap-back voltages will be achieved at higher currents while the opposite is true for lower currents. In summary, the base bias scheme will affect the exponent on the Ic-Vce snap-back boundary curve in Figure 3. Nevertheless, we believe this automated test method still gives us very good and fast limit of the device SOA.

To be able to better compare various epitaxial structures, we further process the measured data and define a model to fit the SOA boundary curve. Using a published analytical model for the onset of the instability boundary [2, 5] is not possible here since we are biasing the device with a fixed base current source. Instead, we determined that a constant power curve fits perfectly our measured SOA (Eq. 1).

$$J_{ce}\left(\frac{mA}{\mu m^2}\right) = \frac{P_{SOA}\left(\frac{mW}{\mu m^2}\right)}{V_{ce}(V)} + \alpha\left(\frac{mA}{\mu m^2}\right) \qquad \textbf{(Eq. 1)}$$

Results from a typical collector design of experiment (DOE) are shown in Figure 4. Here, the collector doping

profiles and thickness were varied to improve the device ruggedness while minimizing the changes to its RF performance.

Although the test tried to match the device current densities based on the initial Gummel sweeps, since we are looking at epitaxial structures that result in different device thermal resistance and device DC gain negative variation with temperature, the measured snap-back points do not line up in the current density scale. This is one more reason for us to model each SOA boundary to be able to compare the structures in a more meaningful way.
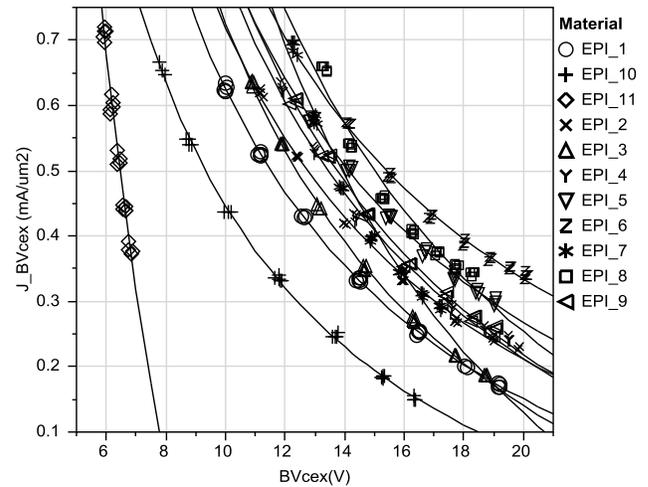

Figure 4. Collector DOE epi structure snap-back loci.

The model curve intercept with Jc=0 is not the same as BVcbo. Figure 5 shows the measured BVceo, BVcbo and the extracted P$_{SOA}$ for these epitaxial structures for quick comparison. The curves intercept with Jc=0 does not correlate with BVcbo; this has no physical meaning since the boundary curve takes the path of the zero base current curve towards the higher collector voltages. Thus, the device will never achieve this condition based on our current bias setup.

The results displayed in Figure 4 are based on epi structures with either uniformly or non-uniformly doped collectors. For uniformly doped collectors, the structures with thicker collectors will show a higher breakdown voltage at lower current densities, while the structures with higher doping will increase the breakdown voltage at higher currents. To further increase the breakdown voltage at higher current densities, the non-uniformly doped structures use a higher doped region closer to the sub-collector, with lower doped regions closer to the base junction. This in effect also limits the decrease in breakdown voltage at lower currents. An example of this structure is EPI_7. This structure shows the highest P$_{SOA}$ among all structures considered in this study.

Aside from the RF figures of merit, power amplifier designers should carefully choose the epitaxial structure for

their designs depending on the mode of operation, given the effective load line, to achieve higher SOA boundaries.
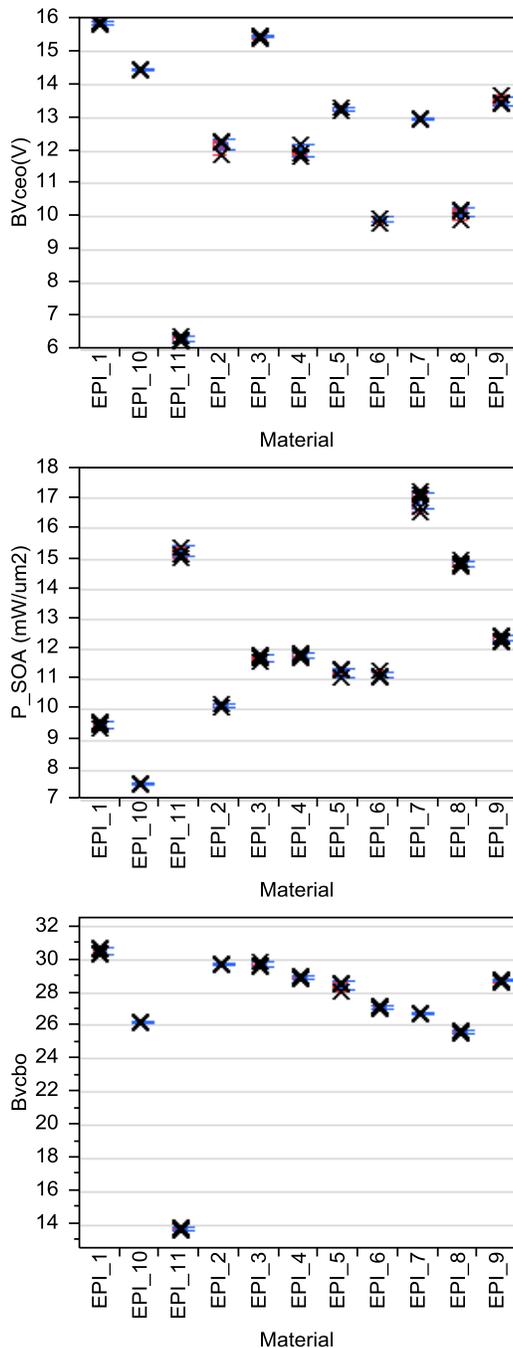

Figure 5. Comparison of collector DOE BVceo, BVcbo, and snap-back parameters.

The fit of the SOA boundary with the constant power curve is impressive, with R^2 values above 0.97. This perfect fit with constant power means this breakdown is mostly thermal in nature, and not voltage breakdown induced. In most HBT devices, the snap-back instability can be caused either by self-heating such as in our case, or by breakdown effect. The balance between the two depends on the specific bias and ballasting conditions. Future work will involve the same tests but with a voltage source Vb to bias the base through various base ballast resistors. These bias conditions would resemble more the conditions for a linear power amplifier. Nevertheless, the current test setup still gives device designers a good understanding of the epitaxial structure's SOA and is a very good tool for collector epi fine tuning.

CONCLUSIONS

In this work we developed a test methodology for high-volume, in-line measurement of device ruggedness. This method is non-destructive and provides accurate results since it monitors both the collector voltage and the collector current beyond the device snap-back in real time during breakdown. This method is useful not only when developing new epitaxial structures for HBT devices, but it also allows us to monitor the device ruggedness in-line for possible deviations due to epitaxial or manufacturing process variations.

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ACRONYMS
HBT: Heterojunction Bipolar Transistor
VSWR: Voltage-Standing-Wave-Ratio
BJT: Bipolar Junction Transistor
SOA: Safe Operating Area
SMU: Source Measurement Unit