High Voltage Capacitors with Increased Lifetimes Using SiN Dielectrics

R. D. Slater

Triquint Semiconductor, 500W Renner Rd, Richardson, TX. 972-994-8514. rslater@tqs.com

Keywords: Capacitor, SiN, dielectric, breakdown, lifetime

Abstract

We present ramped voltage data from a new nitride used in our fabrication process. Using the same fabrication flow, we measured increased lifetimes for capacitors using this new dielectric. Using the linear field model, this translates into capacitors that can sustain higher applied voltages before they fail.

INTRODUCTION

GaAs and GaN MMIC circuit fabrication processes include multiple layers of dielectric and metal interconnects. In recent years the trend for MMIC devices has been to operate at higher and higher voltages. As the input voltage for a MMIC increases, the demands upon the passive elements become higher. One of the issues that needs to be addressed is how to push capacitor operation to higher operating voltages.

Time Dependant Dielectric Breakdown holds that a capacitor (in particular the dielectric) can only pass a fixed charge before it suffers catastrophic breakdown [1]. Thus as the voltage is increased across a capacitor, its lifetime will decrease. Using higher input voltages will then have a direct negative impact on capacitor lifetime. If that lifetime becomes short enough it can compromise the operation of the entire MMIC.

To address this issue, we looked at new nitrides deposited under alternate conditions to improve our capacitor lifetime. Using the widely accepted ramp voltage method [2], we gathered data on similar thickness capacitors using this new nitride and compared it to the original published results to show the improvement [3].

FABRICATION AND TEST SETUP

The fabrication of the capacitors measured in this paper is identical to our previous published work [3, 4]. Again 3 different thicknesses of capacitors were used, named after the nominal dielectric thickness (in nanometers): "CT50", "CT200", and "CT250".

TABLE I
DIFFERENT CAPACITOR TYPES

Type	Bottom Plate	Dielectric	Top Plate
CT50	Metal 0	Nitride 1	MIM
CT200	MIM	Nitride 2	Metal 1
CT250	Metal 0	Nitride 1+ Nitride 2	Metal 1

Metal 0 and MIM are deposited via evaporation and are metal stacks composed primarily of Au. Metal 1 is an electroplated Au layer. Nitride is again deposited by PECVD, but in an alternative reactor than our previously described work, notably a with higher deposition temperature.

The same test array described previously was again used to fabricate devices for test. The top capacitor plate is 100 x 100 μm. The bottom plate is extended by 2 um from the top plate according to TriQuint design rules. Measurements were performed at room temperature and taken from all portions of the fabricated wafer.

Capacitors were tested by applying a voltage from the bottom plate to the top plate which was increased at 2 different rates for both positive and negative potentials. (±4.0 V/s, and ±0.4 V/s). The ramp is approximated by voltage steps of 0.25 V. A capacitor is held to have broken down when the measured current exceeds 10 mA.

A total of 4 wafers were fabricated for this test (from 2 separate lots). Wafers 1 and 2 were run separate from wafers 3 and 4 to gauge repeatability over time. Each test consisted of 24 samples from a wafer for a total of 96 total data points for each capacitor type, polarity, and ramp rate. Each capacitor type is represented by 384 samples that were measured under the various conditions.

Table II and III list the mean and standard deviation for each type of capacitor, both polarities, and both ramp rates. We note again that a negative bias on the top plate causes the breakdown voltage to be higher than if a positive bias is applied. Particularly for the negative bias, some CT200 and most CT250 did not breakdown when the limits of the test equipment (200 V) were reached. We do not list the standard deviation of the CT250 for the reason that most

TABLE II
AVERAGE BREAKDOWN VOLTAGE FOR RAMP TESTS

Wafer	CT50	CT200	CT250	Polarity	Ramp Rate
1	46.3	163.3	199.5*	+	4.0 V/s
2	46.5	161.4	199.8*	+	4.0 V/s
3	44.6	163.6	200*	+	4.0 V/s
4	44.9	165.4	200*	+	4.0 V/s
1	-48.4	-198.4	-200*	-	4.0 V/s
2	-48.8	-197.6	-200*	-	4.0 V/s
3	-45.6	-196.3	-200*	-	4.0 V/s
4	-46.6	-197.0	-200*	-	4.0 V/s
1	42.2	149.3	190.5	+	0.4 V/s
2	43.4	147.9	188.0	+	0.4 V/s
3	42.2	150.9	190.4	+	0.4 V/s
4	41.4	151.9	190.1	+	0.4 V/s
1	-44.8	-187.2	-200*	-	0.4 V/s
2	-44.2	-184.6	-200*	-	0.4 V/s
3	-43.2	-183.6	-200*	-	0.4 V/s
4	-43.1	-183.0	-200*	-	0.4 V/s

*Contains data that exceed test equipment limits

TABLE III
STANDARD DEVIATION OF DATA

Wafer	CT50	CT200	Polarity	Ramp Rate
1	1.8	6.5	+	4.0 V/s
2	1.9	5.0	+	4.0 V/s
3	1.8	2.0	+	4.0 V/s
4	1.4	2.0	+	4.0 V/s
1	2.0	2.8	-	4.0 V/s
2	1.1	3.9	-	4.0 V/s
3	4.4	4.5	-	4.0 V/s
4	1.5	2.5	-	4.0 V/s
1	0.7	4.4	+	0.4 V/s
2	0.6	4.2	+	0.4 V/s
3	0.8	4.7	+	0.4 V/s
4	0.8	2.1	+	0.4 V/s
1	1.4	4.9	-	0.4 V/s
2	2.0	5.8	-	0.4 V/s
3	0.5	2.1	-	0.4 V/s
4	1.2	2.9	-	0.4 V/s

(>90%) did not break down significantly distorting the standard deviation.

There was a single outlier on wafer 3 for the CT50 fast 4.0 V/s breakdown test (demonstrated by elevated standard deviation.) Without this single point, the standard deviation would be 1.6, in line with the other data. Overall the data samples followed a Gaussian distribution for each wafer.

LIFETIME PREDICTIONS

We use the linear field model to predict capacitor lifetime based on ramp voltage data. Previous work has shown that while the linear field model may underestimate lifetime for low applied voltage, it fares well at higher applied voltage [3, 5]. Using this model the time to failure, t(F), is given by:

$$t(F) = t(0)\exp\left[\gamma(E_F - E_A\right]$$

where

$$t(0) = \frac{\Delta t}{1 - \exp\left(-\gamma \Delta E\right)}$$

Δt is the ramp step time, ΔE is the field step in the ramp program, and E_F is the field at failure. E_A represents the applied field for a constant voltage test.

The acceleration parameter is γ, which is obtained by comparing the breakdown field from 2 different voltage rates:

$$\gamma = \frac{ln\frac{R_1}{R_2}}{E_1 - E_2}$$

Using the values obtained from Table II, we can calculate the lifetime in relation to a constant applied voltage. Figure I shows a comparison of the previous published data and the current capacitor dielectric for a CT200 at positive polarity.

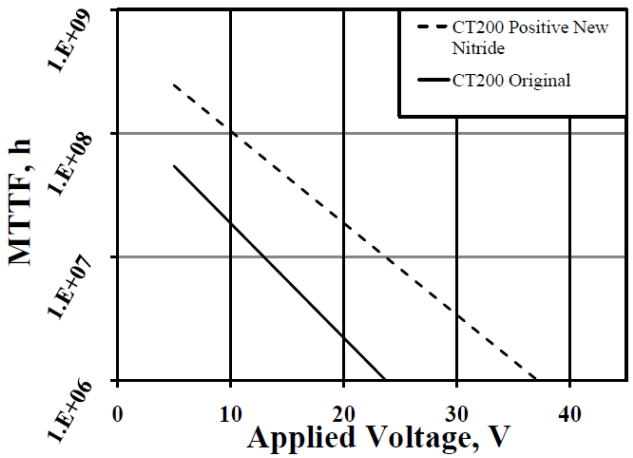

Figure I: MTTF as a function of a constant input applied voltage

Using 10^6 hours as a reference line, we conclude that our new nitride is able to withstand nearly twice the applied voltage for a comparable amount of time as the original nitride. Similar results are found for other capacitors using this nitride and are listed in Table IV.

TABLE IV
COMPARISON OF OLD NITRIDE AND NEW NITRIDE, APPLIED VOLTAGE FOR MMTF OF 10^6 HOURS

Type	Polarity	Previous	New
CT50	+	7.5	13.1
CT50	-	-10.0	-13.2
CT200	+	23.7	37.1
CT200	-	-52.3	-77.3
CT250	+	45.2	56-106*
CT250	-	-79.9	

*Estimate using previous γ range of 27 to 44 nm/V [3].

With the exception of CT50 in the negative polarity, we see a large increase in the applied voltage. We attribute this to the very small γ found for CT50 for negative polarity (32 nm/V) and the sensitivity of the lifetime to very small changes in parameters. However, this is also within the range of previous reported γ for this type of work [3,6,7].

We do note the sensitivity of the lifetime to input parameters. For instance a drop in the mean of 1 wafer for CT50 by 1 V would cause the applied voltage for 10^6 hours to increase from 13.2V to 15.5 V. But given such sensitivity to small changes are we justified that our shift is real? We find that the means of the two different types of nitrides are separated by at least 5 standard deviations (excluding the CT250 as those samples did not fail and thus an accurate mean is unavailable at this point). So while the magnitude of the change may be uncertain, we feel the data strongly suggests an increase in breakdown voltage and thus lifetime of the capacitor. To accurately quantify the change,γ should be as accurately measured as possible, perhaps requiring additional tests at other ramp rates.

We also estimate that the thickness of the dielectric is unchanged from our previous work, but due to differences in the nitride, particularly the etch rate of the dielectric during seed layer deposition (which removes 20% of the overall thickness of the dielectric) for electroplating, this may not be true.

Additionally, the three positive polarities show a larger percent gain than the two negative polarities. This could be a clue as to the difference between the positive and negative breakdown difference and merits further study.

Also our CT250 capacitors failed only on the slow ramp, and thus the gamma from previous work was used. No CT250 capacitors in a negative polarity suffered a breakdown during testing, so we can only estimate what the new values may be.

CONCLUSIONS

We have presented data that demonstrates increased lifetime for higher applied voltage in MIM capacitors for GaAs and GaN technologies. The gain in applied voltage for a lifetime of 10^6 hours was substantial in all but the CT50 negative polarity case. We attribute the difference in the CT50 to an abnormally small measured γ which may be due to difficulties in calculating the acceleration parameter accurately.

ACKNOWLEDGEMENTS

The authors would like to thank G. Drandova and K. Salzman for their helpful guidance, S. Bell for test assistance and the manufacturing team at TriQuint Texas who fabricated the devices.

REFERENCES

[1] B. Yeats, *Assessing the Reliability of Silicon Nitride Capacitors in a GaAs IC Process*, IEEE Transactions on Electron Devices, Vol. 45, No. 4, p. 939, April 1998.

[2] A. Berman, *Time-zero dielectric test by a ramp method*, 1981 Int. Reliability Physics Symposium, p. 204. 1981.

[3] J. M. Beall, K. D. Decker, K. A. Salzman, and G. I. Drandova, *Silicon Nitride MIM Capacitor Reliability for Multiple Dielectric Thicknesses*, 2002 MANTECH Technical Digest, p. 145, 2002.

[4] C. F. Campbell and J. M. Beall, *Design and performance of a highly integrated wideband active downconverter MMIC,* 2001 Radio Frequency Integrated Circuits (RFIC) Symposium Digest, pp. 245-248, May 2001.

[5] G. I. Drandova, J. M. Beall, and K. D. Decker, *SiN Capacitors and ESD*, 2006 MANTECH Technical Digest, p. 83, 2006.

[6] H. C. Cramer, J. D. Oliver, and R. J. Porter, *Lifetime of SiN Capacitors Determined from Ramped Voltage and Constant Voltage Testing*, 2006 MANTECH Technical Digest, p. 91, 2006.

[7] Sefa Demirtas, Jesus A. del Alamo, Donald A. Gajewski, Allen Hanson, *Lifetime Estimation of Intrinsic Silicon Nitride MIM Capacitors in a GaN MMICProcess*, 2009 MANTECH Technical Digest, 2009.

ACRONYMS

TDDB: Time dependant dielectric breakdown
MTTF: Mean time to fail
SiN: Silicon Nitride (Si_3N_4)
MMIC: Monolithic microwave integrated circuit