Wafer Level Bump Technology For III-V MMIC Manufacturing

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Abstract

Wafer level bump technology that is compatible to III-V MMIC technology is reported. Two different wafer level bump technologies are presented in the paper. One is solder ball bump and the other is copper bump. Both are fully compatible with existing III-V MMIC backside manufacturing processes. Silicon nitride, deposited at room temperature, is used as solder mask and shows excellent solder blocking capability. UBM (Under-Bump-Metallization) materials were specially selected for their solid diffusion barrier characteristics and strong adhesion between bump and MMIC backside metal pad. Bump planarity, shear strength and solderability are extensively characterized, and benchmarked with industry specifications

INTRODUCTION

Flip-chip technology has gained attention in III-V compound semiconductor community as people look towards replacing traditional wire bonding technology to enhance MMIC module functionality and reducing the cost of manufacturing. As frequency of micro wave communication continues to increase and I/O pitch size approaches wire bonding limitations, the need for a wire bonding free packaging technology dominates other concerns [1][2]. As 3D wafer level packaging technology becoming available and important to RF MMIC applications, so is the need for developing quality high density bumps to attach 3D chips to the board. [3].

Wafer level bump technology for silicon semiconductor technology has been widely studied and implemented in the modern semiconductor industry, but the III-V MMIC industry has lagged due to the unique characteristics of its fabrication process. Special bump materials and processes have to be developed to fit into the conventional MMIC wafer backside process flow. This paper examines a few key challenges in developing a bump technology that is compatible with existing MMIC backside process. Two advanced bump techniques tailored for MMIC manufacturing have been demonstrated.

KEY CHALLENGES TO INTEGRATE WAFER LEVEL BUMP INTO MMIC BACKSIDE PROCESS

A typical III-V compound semiconductor backside process starts with thinning a wafer mounted on a rigid sapphire carrier, to the thickness necessary for the designed RF performance. In most cases this is a few micro inches, which can make a GaAs or InP wafer extremely fragile to handle. Any attempt to apply bumps on these wafers after normal backside processing and wafer demount would take a significant yield loss due to wafer breakage

The bonding material used to mount the wafer on rigid sapphire carrier for backside process is typically made of soft cured polymer with polymerization temperature of less than 200 degrees. This limits the availability of suitable solder mask materials. The most common solder mask employed for silicon flip-chip technology is a hard cured polymer, like polyimide or BCB, cured at a temperature of much higher than 200C.

Unlike silicon chips that typically use Al pad for connections, Au pads are the default configuration for III-V compound semiconductor MMIC chips. To inhibit the well-documented formation of Au-Sn intermetallics, the desired UBM material has to exhibit excellent diffusion barrier capability and good solderability to create robust mechanical joints that do not suffer from long term reliability degradation.

RESULTS

Figure 1 illustrates the process integration flow to fabricate bumps at the wafer level. Two bumping methods are studied: Tin/Lead solder ball bump and copper stud bump. The advantage of solder ball bump is its process maturity and wide adoption among industries. While the newly emerged copper stud bump significantly boosts MMIC module performance by offering excellent thermal and mechanical joints between the chip and board.

Figure 2 shows a copper bump array with a Sn/Pd solder cap on a GaAs MMIC wafer. The high across-wafer uniformity of the plating rates for both copper and solder cap enables excellent bump planarity within chip and from chip to chip, which is essential for chip attachment yield and quality.

Figure 3 demonstrates a solder ball array on a GaAs MMIC wafer. The original diameter of the solder balls is 5 micro inch. After it is placed on the pad using a solder ball laser placement machine, the ball collapses slightly and settles at a pad size dependent height. The ball shape is typically recovered by subsequent reflow processes.

CONCLUSIONS

Two fully compatible wafer level bump techniques, copper stud bump and Sn/Pd solder ball bump, have been successfully integrated into an existing III-V MMIC backside process. Superior characteristics from both bumps have been demonstrated. This process enables both chip level and wafer level assembly for III-V MMIC industry to reduce the cost of process ownership and enhance RF performance.

REFERENCES

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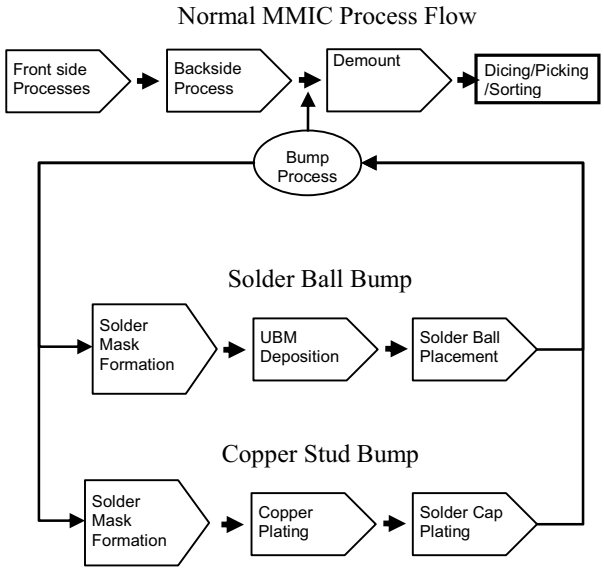

Figure 1 Wafer Level Bump Integration Process Flow

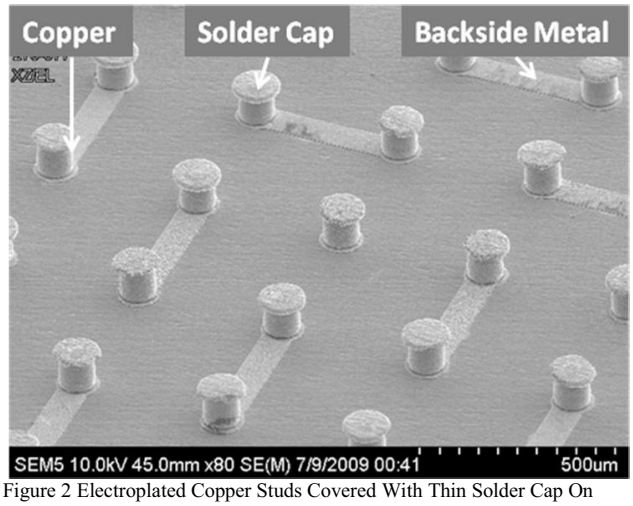

Figure 2 Electroplated Copper Studs Covered With Thin Solder Cap On Top of GaAs Wafer Backside Metallization. Total bump height 100um

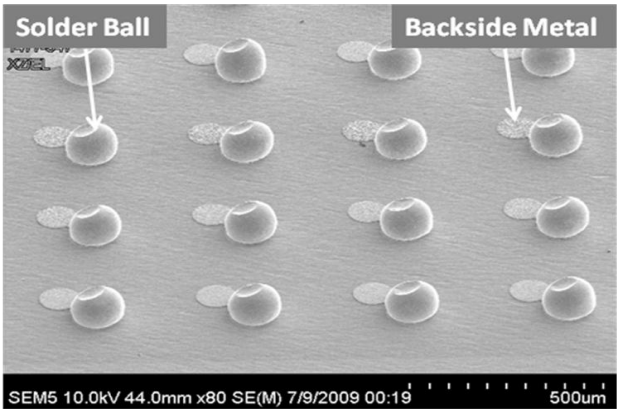

Figure 3 Solder Ball Array On Top Of GaAs Wafer Backside Metallization. Final ball height is about 90um