

Improved Emitter Resistance Through the Use of Barrier Metals

Alan Bratschun and T.C. Tsai

Avago Technologies, Fort Collins, CO, USA, alan.bratschun@avagotech.com, (970)288-2119
WIN Semiconductors, Tao Yuan Shien, Taiwan, tctsai@winfoundry.com, (03)397-5999 Ext 1533

Keywords: emitter, contact, titanium, tungsten, HBT

Abstract

In this paper we report the improvement of emitter series resistance for InGaP HBT transistors using barrier metals in the contact layers. To demonstrate the improvement a simple baseline process, using a thick titanium contact layer, is compared to processes using a barrier layer of either tungsten or titanium tungsten. Although each of these emitter contact schemes produces a non-alloyed ohmic contact, and does not require exposure to high process temperatures, processing above 300 °C is unavoidable in the integrated process. Trend charts show reduced emitter resistance and better uniformity over multiple lots. High resolution STEM images exhibit the absence of physically degraded interfaces. Additional data, not presented in this paper, has shown that improved emitter contacts are beneficial to the reliability of HBT power amplifiers.

INTRODUCTION

Low and consistent emitter contact resistance is critical in HBT processes to produce efficient, well matched, devices. In addition to intended sources of emitter resistance, such as heterojunction interfaces or lightly-doped GaAs layers used to form ballast resistors; the metal contact to the semiconductor is a source of resistance. Highly doped, low band gap material, such as InGaAs, is used to ensure an ohmic contact to the semiconductor. With an InGaAs layer, most metals can be used to form an ohmic contact. The choice of metal will affect the simplicity of the integrated process and the reliability of the devices.

For this work, we report the total emitter series resistance as measured with the flyback technique [1]. Here, the emitter is grounded and current is forced into the base. The open circuit collector voltage is measured. The emitter resistance is taken as the slope of the linear segment of the curve (see Fig 1).

Using the flyback resistance to monitor contact resistance has several advantages. The flyback resistance parameter includes all components of series resistance, including contact resistance, and can conveniently be measured on various size HBT devices. This proved to be valuable for this study because, although contact degradation

can be seen on all size devices to some degree, it is more consequential on devices with smaller emitter area.

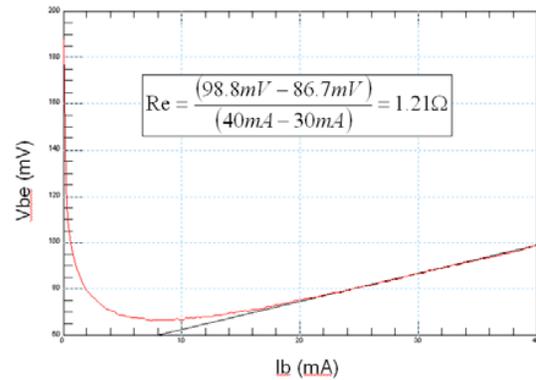


Figure 1: Emitter resistance using flyback measurement

Titanium (Ti) adhesion layers for use with tungsten (W) contacts were proposed in a self-aligned HBT structure for base and emitter contacts in 1992 by Lee [2]. Although these contacts gave low resistance with process temperatures up to 380c, long-term reliability was not reported and the resistance was found to drop with current stress. Wakita reported that the use of Ti to contact InGaAs emitter layers can lead to poor contacts [3]. It was reported that use of thick, 50 nm, Ti would lead to degraded contacts. In this work, it has been confirmed that using thin Ti layers, down to 5 nm, lowers the emitter resistance (see figure 2); however, this improvement could not be realized for integration reasons. For high power devices, Liu has stated that refractory metals including W, TiW, or WSi result in more reliable contacts [4]. Chor reported the use of a thin W barrier layer for base contacts to InGaAs bases in 1996[5], which gave stable contact performance with anneal temperatures up to 400 °C.

EXPERIMENT

An internal InGaP HBT process with a commonly reported emitter contact structure was used to demonstrate the reduction of emitter resistance. The semiconductor layers included, starting from the surface, a heavily doped cap InGaAs layer, a graded InGaAs layer, and a low resistivity silicon doped GaAs buffer layer. The cap layer was 45 nm thick and doped at greater than $2 \times 10^{19} \text{ cm}^{-3}$.

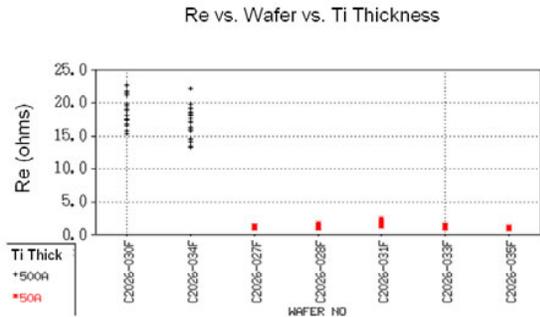


Figure 2: Emitter resistance improvement with 5 nm Ti layer.

The benchmark process included a silicon nitride coating over the emitter into which contact openings were etched. The standard contact metal consisted of stacked layers of titanium, platinum, and gold. The titanium thickness was varied, but was generally greater than 20 nm.

The experiment includes adding a sputtered barrier layer of either TiW or W between the InGaAs and the Ti layers.

RESULTS

Cross sectional STEMs were taken of the emitters after complete processing, including thermal cycles, to evaluate the physical stability of the interfaces. Figure 3 shows the appearance of the emitter with titanium directly contacting the InGaAs. The interface is rough containing voids and intermetallic compounds. Figure 4 shows the interface with a 20 nm W barrier layer added between the titanium and the InGaAs layer. The interface is well formed and stable. Figure 5 shows the interface with a 20 nm layer of titanium tungsten between the titanium and the InGaAs layer. There were no intermetallic compounds or voids detected.

The base-line process was eventually changed to add a barrier layer as standard practice and additional trend data was collected (see fig 6). The mean flyback resistance after the change dropped from 27.6 ohms to 1.96 ohms, and the standard deviation of the resistance dropped from 33.7 ohms to 0.18 ohms.

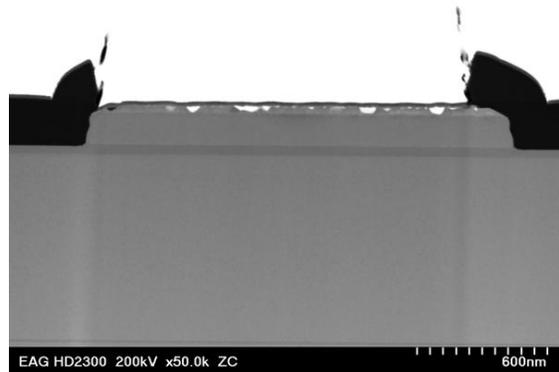


Figure 3: Emitter Contact: 20 nm Ti, with no barrier layer. Note rough, degraded interface.

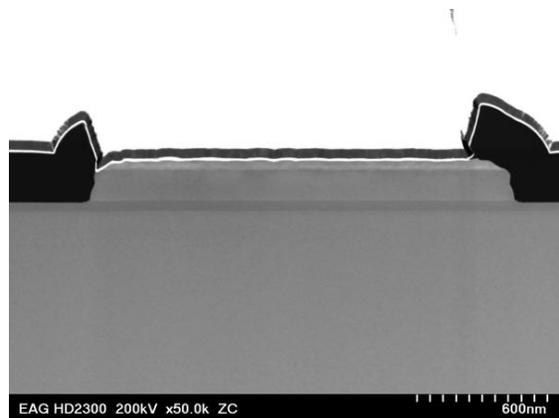


Figure 4: Emitter Contact: 50 nm Ti with 20 nm W barrier layer.

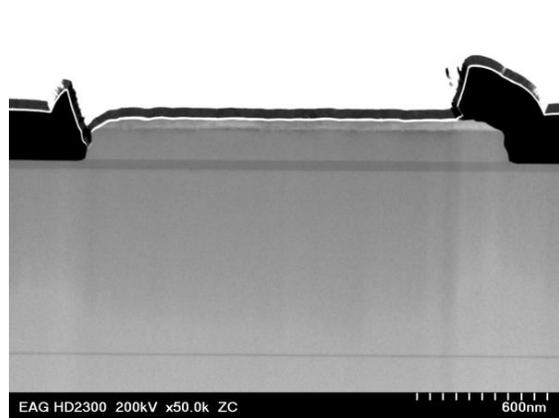


Figure 5: Emitter Contact: 50 nm Ti with 20 nm TiW barrier layer.

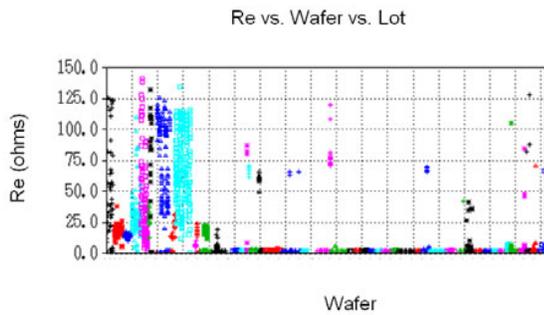


Figure 6: Improvement in emitter resistance trend with added barrier layer.

CONCLUSION

The addition of refractory barrier layers as part of the emitter contact can result in a more stable interface with substantially reduced resistance and less variability in resistance.

ACKNOWLEDGEMENTS

The authors would like to recognize the expertise of Robert Long in developing the processes used to fabricate the devices reported in this experiment. Tim Valade provided the various metal layers that were studied. The work benefited greatly from informal conversations with Hans Rohdin and Steve Kofol covering semiconductor contact physics and technology. Royce Gover and Osvaldo Buccafusca also enabled this work by developing the needed test algorithms.

REFERENCES

- [1] L. J. Giacoletto, *Measurement of Emitter and Collector Series Resistances*, IEEE Trans, ED-19, pp. 692-693, 1972
- [2] W. Lee., T. Enoki, S. Yamahata, Y. Matsuoka, T. Ishibashi, *Submicrometer Self-Aligned AlGaAs/GaAs Heterjunction Bipolar Transistor Process Suitable for Digital Applications*, IEEE Trans on Elect. Dev. Vol. 39, No. 12, pp. 2694-2700, Dec 1992
- [3] A. S. Wakita., N. Moll., S. J. Rosner, A. Fishcer-Colbrie, *Thermal Stability of MoAu and TiPtAu Nonalloyed InGaAs Contact*, J. Vac. Sci. Technol. B 13(5), pp. 2092-2098, Sep/Oct 1995
- [4] W. Liu, *Fundamentals of III-V Devices HBT's, MESFETS, and HFETs/HEMTs*, John Wiley and Sons, Inc., p.458, 1999
- [5] E. F. Chor, R. J. Malik, A. Hamm, R. Ryan, *Metallurgical Stability of Ohmic Contacts on Thin Base InP/InGaAs/IP HBT's*, IEEE Elec. Dev. Ltrs., Vol. 17, No. 2, Feb. 1996, pp. 62-64

ACRONYMS

HBT: Heterojunction Bipolar Transistor
 InGaP: Indium Gallium Phosphide
 InGaAs: Indium Gallium Arsenide
 WSi: Tungsten Silicide
 STEM: Scanning Transmission Electron Microscopy