Enhancement-mode Pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with InAlP Native Oxide Gate Dielectric

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Abstract

As an alternative to conventional III-V HEMTs and MESFETs for high-speed and wireless applications, enhancement-mode pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with an ultra-thin InAlP native oxide gate dielectric are reported. The gate dielectric is formed by wet thermal oxidation of a 2 nm InAlP epitaxial layer, resulting in a 3.5 nm thick InAlP oxide gate dielectric. The gate oxide reduces the gate leakage below that of HFETs based on the same epitaxial structure by more than 10^5 times. A typical 0.5 µm gate length device exhibits a threshold voltage of 1.05 V, a peak extrinsic transconductance of 146 mS/mm, and a saturation drain current density of 95 mA/mm. A cutoff frequency, f_T, of 34 GHz, and a maximum frequency of oscillation, f_{max}, of 49 GHz have also been achieved. These results suggest that RF applications could benefit from III-V MOSFETs with native oxide gate dielectric.

INTRODUCTION

III-V channel MOSFETs are potentially attractive device candidates for use in future high-speed and RF circuits as an alternative to MESFETs or HEMTs. For enhancement-mode devices, replacing the Schottky gate contact with an insulating metal-oxide-semiconductor structure can result in increased allowable gate voltage swing, while at the same time suppressing gate current due to the higher effective gate potential barrier. Since the use of enhancement mode devices enables the design of circuits operating from a single power supply, this advantage is particularly attractive for battery-powered and mobile RF devices.

The historical difficulties in developing III-V MOSFETs are well known; studies of native oxides of III-V semiconductors, e.g. GaAs, have often shown a high interfacial trap density (see e.g. [1]) and a strongly pinned Fermi-level at the oxide/semiconductor interface (see e.g. [2]). However, recently several dielectrics on GaAs or $In_xGa_{1-x}As$ have been reported to produce promising device performance, including atomic layer deposition (ALD) grown Al_2O_3 [3], [4], molecular-beam epitaxy (MBE) grown $GdGaO/Ga_2O_3$ [5], and wet thermally oxidized InAlP [6]. Each appears to offer promise for advancing the performance of III-V MOSFETs. The use of thermally-oxidized InAlP as the gate dielectric offers advantages in terms of fabrication flexibility [6]. In this approach, InAlP oxide is formed as a process step from epitaxially-grown InAlP, and thus no special surface passivation, cleaning, or post-growth gate dielectric deposition steps are required. In addition, a Si-like inward diffusion of oxygen dominates the kinetics of oxide growth, providing a clean oxide-semiconductor interface [7]. The excellent electrical and insulating properties of wet thermal oxides of InAlP [8], [9] have been confirmed by previously demonstrated enhancement-mode [10] and depletion-mode GaAs-channel MOSFETs [6], [11], [12].

In this paper, we report enhancement-mode pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with an ultrathin InAlP native oxide of 3.5 nm as the gate dielectric. A threshold voltage of 1.05 V was obtained, as well as the highest cutoff frequency, f_T, for III-V channel MOSFETs at 0.5 µm gate length, of 34 GHz. The device fabrication and prospects for further performance improvement are also presented.

DEVICE STRUCTURE AND FABRICATION

The epitaxial heterostructure for the devices presented here (shown in Figure 1) was grown by molecular beam epitaxy (MBE). The structure consists of a pseudomorphic undoped $In_{0.22}Ga_{0.78}As$ channel, an undoped $In_{0.5}Ga_{0.5}P$ layer that serves as both a spacer and oxidation stop layer, a 20 Å n^+-InAlP layer lattice matched to GaAs, and a 250 Å heavily doped GaAs cap.

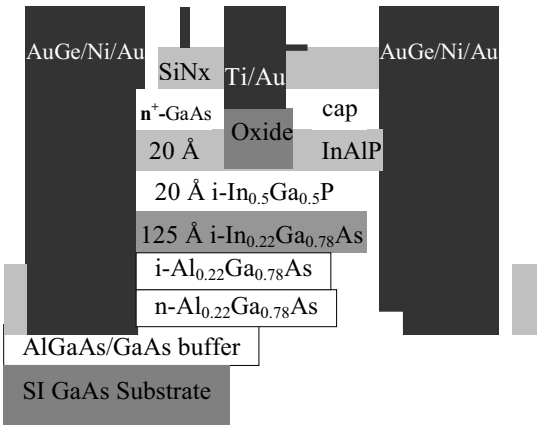

Figure 1. Cross-sectional schematic diagram of a pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFET with InAlP native oxide.

Device fabrication included mix and match optical/electron beam lithography to define the device geometries, AuGe/Ni/Au source and drain metallizations, and Ti/Au gates [6]. After device isolation by wet chemical etching, a thin layer of SiN_x was deposited by plasma enhanced chemical vapor deposition (PECVD) to assist a T-gate process used to self-align the gate recess etch, the InAlP oxidation region, and the gate foot metallization in order to minimize series resistance. As indicated in the cross-sectional TEM image in Figure 2, only the InAlP directly beneath the gate foot is oxidized during a 9.5 min wet thermal oxidation at 440 °C; the InAlP in the source/drain access region remains as semiconducting n^+ InAlP. The thickness of the oxide is measured to be approximately 3.5 nm, as inferred from variable-angle spectroscopic ellipsometry (VASE). Following the AuGe/Ni/Au metallization and thermal annealing of the source and drain contacts, the device was completed by defining the gate "head" pattern using electron beam lithography and lift-off of Ti/Au as the gate metal. As shown in the TEM image in Figure 2, the gate head is supported by SiN_x and makes direct contact to the gate oxide in the gate foot region. This quasi-self-aligned gate metallization and regional oxidation reduces the lateral access resistance to enable high RF performance.

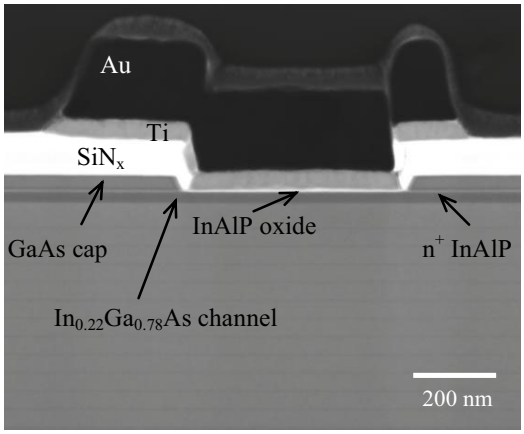

Figure 2. Cross-sectional TEM image for a pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFET with 3.5 nm InAlP native oxide at L_g=0.5 μm.

DEVICE PERFORMANCE

Both the dc and RF performance have been characterized for the fabricated pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with wet thermal native oxide of InAlP as the gate dielectric.

A 3.5 nm InAlP wet thermal oxide results in a typical MOSFET gate leakage current that is 10^5 times smaller than that of a comparable HFET based on the same epitaxial structure, as shown in Figure 3. This gate leakage reduction is a major advantage of MOSFETs over Schottky-gated devices, and allows operation at much higher gate biases than is possible with conventional HFETs.

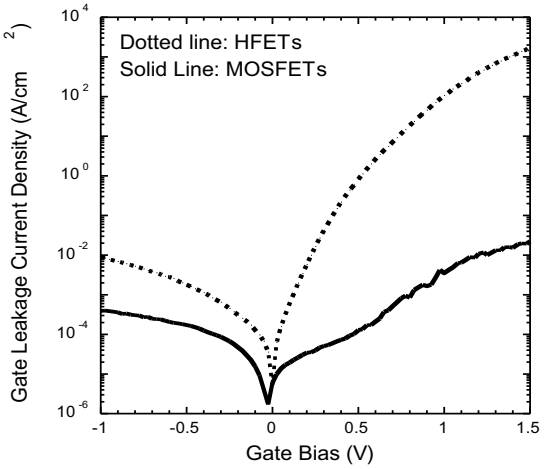

Figure 3. Typical gate leakage current comparison of $In_{0.22}Ga_{0.78}As$-channel MOSFETs with native InAlP oxide gate dielectric and HFETs based on the same epitaxial heterostructure.

A typical measured common-source transfer characteristic for a device with a 0.5 μm gate length and a 100 μm gate width is shown in Figure 4. The device operates in enhancement mode with a threshold voltage of +1.05 V (determined by linear extrapolation of the drain current from peak g_m), a peak extrinsic transconductance of 146 mS/mm and saturation drain current density of 95 mA/mm.

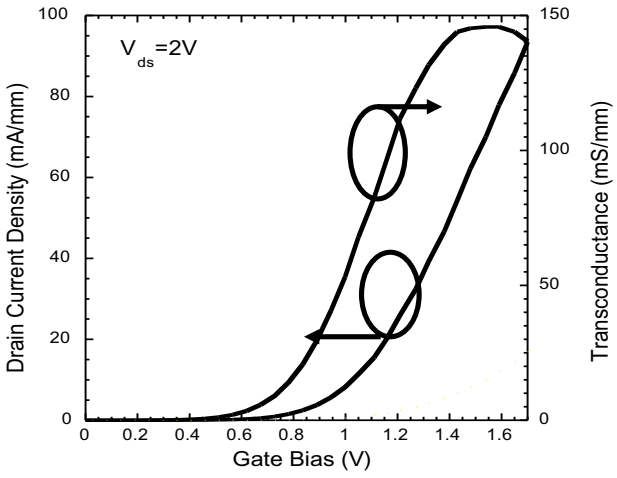

Figure 4. Measured common-source transfer characteristics for a pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFET with InAlP oxide at L_g=0.5 μm.

The measured common-source characteristics are shown in Figure 5. The characteristics show clear pinch-off at gate voltages below 0.6 V and no significant contribution to drain current from the gate at V_{gs} up to 1.7 V.

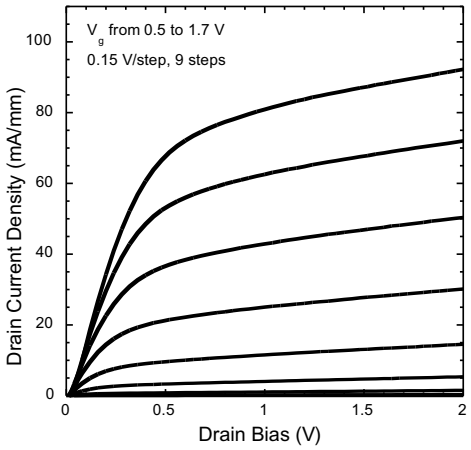

Figure 5. Common-source current-voltage characteristics for a pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFET with InAlP oxide at L_g=0.5 μm.

On-wafer S-parameter measurements for 1-40 GHz were used to assess the microwave performance. The peak current gain cutoff frequency, f_T, and corresponding maximum frequency of oscillation, f_{max}, were extracted. At V_{ds} = 2 V and V_{gs} = 1.5 V, an f_T of 34 GHz and an f_{max} of 49 GHz were obtained by extrapolation of the current gain (h_{21}) and maximum available gain (MAG) as plotted in Figure 6. This is the highest value reported for either depletion or enhancement mode III-V channel MOSFETs at this gate length [5].

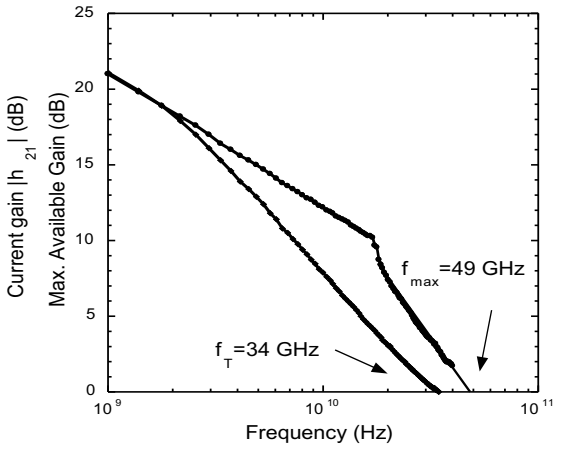

Figure 6. Measured microwave performance for a pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFET with InAlP oxide at L_g=0.5 μm.

Previously reported enhancement-mode GaAs-channel MOSFETs with native InAlP oxide gate dielectric thicker than 10 nm demonstrated an extrinsic peak transconductance of 24.2 mS/mm and a saturation drain current density of 63.8 mS/mm [10]. The pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs reported here with much thinner InAlP oxide gate dielectric exhibit a substantial performance improvement, even at this early stage of development.

CONCLUSIONS

Enhancement mode pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with ultrathin InAlP native oxide gate dielectric have been fabricated. The devices exhibit a threshold voltage of 1.05 V and a cutoff frequency of 34 GHz with a 0.5 μm gate length, and clearly show the promise of InAlP-oxide gate pseudomorphic MOSFETs for single-supply compound semiconductor RF applications. The use of InAlP oxide, formed from wet thermal oxidation of epitaxially-grown InAlP, as the gate dielectric provides substantial process flexibility for realizing compound semiconductor-based MOSFETs. Further investigation of device scaling provides a path for realizing additional performance improvements.

ACKNOWLEDGEMENT

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ACRONYMS

MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
MESFET: Metal Semiconductor Field-Effect Transistor
HEMT: High-Electron Mobility Transistor
HFET: Heterostructure Field-Effect Transistor