GaN-on-Si for Power Conversion

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Abstract

GaN-on-Si has become the most promising technology for next-generation power switching devices to overcome intrinsic Si limits for high temperature operation, high efficiency at high operating voltage, high switching frequency. Besides unique material properties, we show that the design of advanced GaN FET devices for power conversion can be improved thanks to the use of in-situ SiN passivation. This in-situ SiN layer is further shown to be a key parameter for device stability at elevated temperatures, significantly enhancing the device reliability in high temperature accelerated lifetime tests. We review herebelow the demonstration of depletion and enhancement-mode devices with breakdown voltages above 600V with already more than an order reduction in conduction loss compared to most advanced Si MOSFETs, and able to operate under higher switching frequencies.

I. Introduction

Power electronics for generating and converting energy is covering a large range of applications ranging from power supplies for ICTs, to motor drives, solar converters or hybrid electrical vehicles. Developing the next generation of power components will require the use of III-Nitride semiconductors: they exhibit a high breakdown voltage due to the high field strength (~ 3.5 MV/cm), which is an order of magnitude better than Si. Additionally, very low on-resistance and high switching speed can be obtained due to the two-dimensional electron gas (2DEG) of the AlGaN/GaN heterostructure which exhibits high mobility and large carrier concentration. Finally, the wide band-gap properties also enable operation at high temperature. However, the key criterion for market adoption will remain cost: this wide band gap material is the sole to offer a reasonable market perspective in terms of cost/performance ratio, due to the unique possibility to grow advanced heterostructures on large diameter Si substrates, up to 150 mm and, in a near future, 200 mm. Additionally, the possibility to develop a process compatible with CMOS standard technology opens very good perspective in further cost reduction by leveraging on Si economy of scale.

While AlGaN/GaN HEMTs are successfully introduced on the market for RF amplification, slightly different device characteristics are required for power conversion. The breakdown voltage must typically be larger in the off-state than the one required for RF power amplification; still, the specification value significantly depends on the target application and ranges between 100V and 1000V. The other device specifications are defined by the main drivers for replacing Si MOSFETs or IGBTs: typically, reduced specific on-resistance, higher switching frequency, smaller gate capacitance and lower leakage currents at high reverse voltages. Last but not least, beyond demonstrating excellent device characteristics, in-depth reliability studies of III-Nitride switching devices are still required.

II. Heterostructure design and in-situ SiN passivation

The epitaxial layers are grown by Metal-Organic Chemical Vapor Deposition (MOCVD) on 4'' or 6" Si (111) substrates. Two aspects in material growth require utmost attention for real device applications: (1) the stress control in the epilayer, which, if not controlled, leads to wafer crack and/or bow (N.B.: stress control becomes a more and more critical issue, as thicker layers are required for higher breakdown voltages); (2) the control of deep traps, either in the bulk or on the surface. Those traps were well-known in GaN RF power transistors to be responsible for DC-RF dispersion: they would in switching applications dramatically negatively impact the dynamic on-resistance. More details on epitaxial growth can be found in [2].

In order to allow for high voltage operation, instead of using AlGaN/GaN single heterostructures (SH), we are growing Double Heterostructure Field Effect Structures (SiN/AlGaN/GaN/AlGaN - DHFET) [1], as shown in Fig. 1. These structures enhance the confinement of the electrons in the channel and allow to increase the intrinsic breakdown of the epistack from 400V (SH) to 600V (DHFET), for a buffer layer thickness of 2µm on the Si substrates [3]. Appropriate strain engineering allows to deposit more than 4µm thick layers on Si substrates, leading to epiwafers with an intrinsic breakdown voltage higher than 1100V, when measured between two mesa structures, on a floating Si substrate. A typical heterostructure design is shown in Fig. 1: it consists of a 2µm thick AlGaN buffer, a 150 nm GaN channel and 25 nm $Al_{0.35}GaN$ layer , capped by 50 nm of in-situ Si_3N_4.

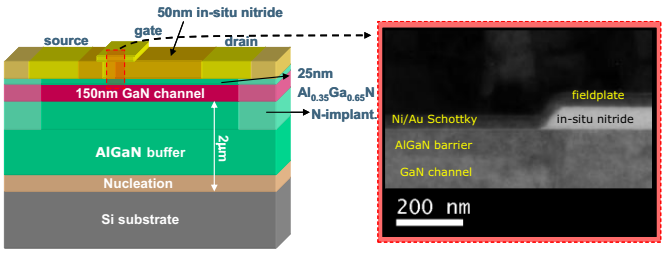

Figure 1: (Left) Schematic of a typical depletion-mode SiN/AlGaN/GaN/AlGaN DHFET; (Right) TEM picture of the slant-edge gate contact, including a field-plate technology, processed by etching in in-situ SiN.

Depending on target device specifications, the heterostructure design may slightly vary (channel thickness, Al composition…). A typical example is shown below for enhancement-mode devices. However, any of our GaN FET devices is capped with an in-situ Si_3N_4 top layer, grown by MOCVD as part of the epi process. Its use has been shown to properly control the filling of the surface states during device operation. Indeed, the SiN is believed to provide enough charge to neutralize the surface charge of the AlGaN barrier layer, so that its surface potential no longer contributes to 2DEG depletion.

In-situ SiN further offers a very interesting tool for developing lower channel resistance and an interesting additional degree of freedom to engineer the top part of the HEMT towards different device specifications. As GaN FETs are lateral devices, reducing the channel conduction loss is actually crucial. In switching applications, Al rich barrier are thus highly desired for increasing the current density in the transistor, as well as for reducing as much as possible the specific on-resistance. We have shown that thanks to SiN cap layer, the Al concentration can be increased without any significant material degradation. Contrarily, in uncapped or GaN-

capped AlGaN/GaN 2DEG, relaxation of the strained top AlGaN layer typically prevents high Al content in the top layer. The use of in-situ SiN capping appears to postpone the relaxation mechanism of the strained AlGaN onto the GaN. We demonstrated $SiN/Al_{0.35}Ga_{0.65}N/GaN/AlGaN$ DHFET with sheet resistance (R_{sh}) well below 300Ω/□ on 100mm and 150mm Si (111) substrates. We have further demonstrated enhancement-mode devices, using Al content as high as 55% [5] or even pure ultra-thin AlN barrier [6]. For a SiN/AlN/GaN/AlGaN DHFET design, the sheet resistance goes down to 355 Ω/sq. for AlN layers as thin as 2nm. This results in high transconductance values even for large gate length, opening new perspectives for high frequency operation. Further taking into account the role played by SiN to neutralize the surface charges, we have proposed an innovative approach to develop enhancement-mode devices, required for power converters, by combining a thin AlGaN barrier layer and local removal of the SiN under the gate, as shown in Figs 3 and 4. This is further discussed below.

The in-situ SiN layer is also shown to be a key parameter for device stability at elevated temperatures, significantly enhancing the device reliability in high temperature accelerated lifetime tests. Figure 2 shows the modification of the Two-Dimensional Electron Gas, measured by Hall measurements, in a high temperature step-stress experiment conducted on three different Van-der-Pauw structures. These structures consisted of a GaN buffer followed by 22nm of AlGaN (35%): the first structure was capped with 3 nm in-situ SiN, the second one with 2 nm GaN cap and the last one was uncapped. The temperature was ramped up from 500ºC to 900ºC every 30 min using a step of 100ºC. Clearly, the uncapped and GaN capped structures show a degradation of the carrier concentration and Hall mobility above 600 ºC.

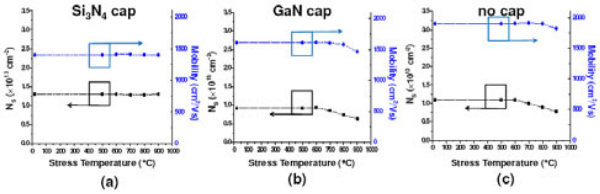

Figure 2: Thermal stability of the heterostructures assessed by Hall measurements on Van der Pauw structures, stored at increasing temperatures for 30 min in steps of 100°C.

As confirmed by TEM and AFM pictures (not shown here), this can be attributed to the relaxation of the top AlGaN layer, which doesn't occur with in-situ SiN capping layer. This will partly explain the excellent device stability at high temperatures of in-situ passivated devices.

III. Device Fabrication: Depletion-mode and Enhancement-mode

Ohmic contacts are first formed using Ti/Al/Mo/Au metal stack followed by Rapid Thermal Annealing at 850°C in N_2 ambient. Device isolation is obtained by high-energy Nitrogen implantation. The gate is then patterned into the SiN, by a plasma etched process based on SF_6, highly selective towards AlGaN. By a reduction of the RF power of the SiN plasma etch from 50 W to 5 W and thus the applied DC bias, implantation of F ions under the gate can be avoided. This, in turn, avoids dispersion and instability of the threshold voltage under thermal or electrical stress. As a result, the threshold voltage is now mainly determined by the design and uniformity of the epitaxial layer stack and the gate length. We are now in a position to define enhancement-mode devices, without any recess in the AlGaN layer [5,6], as shown in Fig. 3. SiN removal under the gate electrode prior to Ni/Au gate metallization (see fig. 3(b)) indeed allows to locally deplete the channel. For an AlGaN layer thickness of 4nm, with Al concentration of 45%, we obtain a normally – off device operation. At the same time, low access resistance in the source-gate and gate-drain areas is maintained as sheet resistance is low in the 2DEG (see fig. 3(a)). Statistical analysis based on measurements of 2100 transistors across a 4" wafer show very narrow distributions for V_T as function of L_G.

A slant gate profile is designed to reduce field effects at the gate edge, as well as a gate connected field-plate. Finally, a second SiN passivation layer is deposited by PECVD. This combination of in-situ passivation, slant etched gate process and ex-situ passivation is a robust approach, which allows to significantly reducing any impact of surface states onto device operation. These dispersion phenomena, typically assessed in nitrides by pulsed IV measurements, are indeed negligible in those devices, as is shown in Fig. 6.

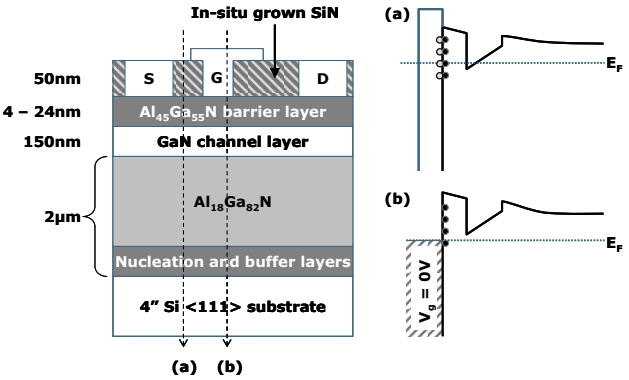

Figure 3: Enhancement-mode devices. Left: Schematic of the device design; Right: Band diagram showing (a) the filling of the 2DEG in access regions and (b) the depletion of the 2DEG in area where the SIN is removed, i.e. below the gate.

IV. Device Results

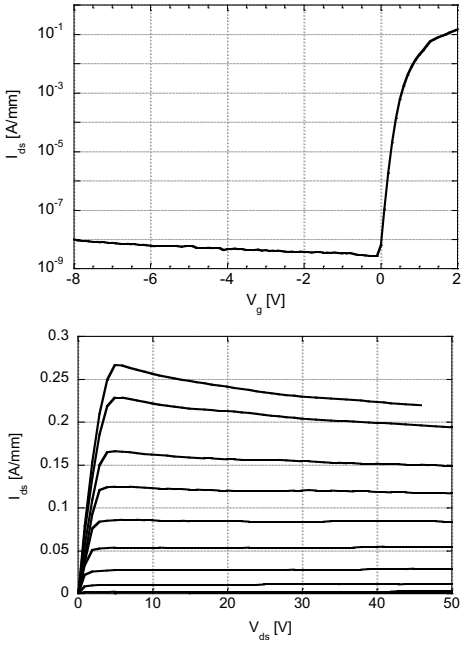

Figure 4: Top: Transfer curve in log scale of a device with L_G = 1.5 µm and L_{GD} = 8 µm on a 4 nm $Al_{45}Ga_{55}N$ layer; Bottom: Output characteristics of a device on a 4 nm $Al_{45}Ga_{55}N$ layer with L_G = 1.5 µm and L_{GD} = 8 µm. V_{GS} is swept down from 2V in 0.2V steps showing the high on/off ratio of over 10^7.

Optimized heterostructures have been used to demonstrate depletion-mode and enhancement-mode devices with breakdown voltage above 1000V. A typical transfer characteristic of an e-mode device, such as described in Fig. 3 with 4 nm of AlGaN 45% is displayed in Fig. 4(a). It has a pinch-off current below 10^{-8} A/mm at V_{GS} = 0 V and V_{DS} = 15 V. The output curves in Fig. 4(b) of the same device indicate a saturation current $I_{DS,sat}$ of more than 0.25 A/mm. The ratio between on-state and off-state drain current is over 10^7. Due to the proximity of the gate to the channel, the maximum transconductance is as high as 210 mS/mm. Transconductance, as high as 315mS/mm, for a gate length of 2 µm, is even achieved with the ultrathin (2nm) AlN barrier [6]. State-of-the-art specific on-resistances ($R_{on,sp}$) either for depletion or enhancement-mode devices have been demonstrated using in-situ SiN passivated devices: for e-mode, $R_{on,sp}$ of 1.25 mΩcm^2 has been measured, associated to breakdown voltages of 580V, or $R_{on,sp}$ as low as 5.5 mOhmcm^2 for a breakdown voltage above 1000V. These values represent more than one order of magnitude reduction of the $R_{on,sp}$ (i.e. conduction losses) compared to the best Si switching devices. Specific on resistance values are typically smaller by a factor 2 for depletion-mode devices compared to enhancement-mode devices. However, as shown in Fig. 5, the device breakdown voltage is independent of the Vt value. We typically define breakdown when a drain leakage current of 1mA/mm is reached. In our case, at 80% of this breakdown voltage, the drain leakage current is around 5 µA/mm. This implies that the hereby reported process can significantly reduce the off-state power dissipation compared to earlier reported approaches. The breakdown voltage increases linearly with the gate-drain distance for small Lgd; however, it saturates to a value defined essentially by the buffer layer thickness, due to breakdown of the Si substrate.

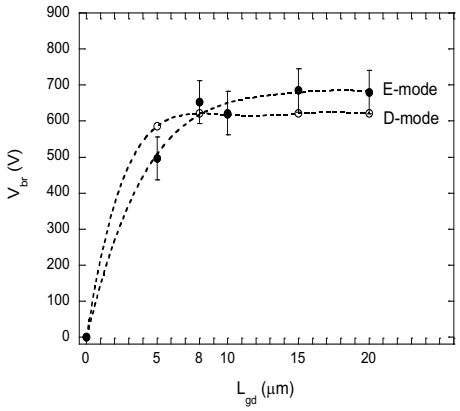

Figure 5: Comparison of breakdown voltages of E-mode (filled circles) and D-mode devices (open circles) with the same buffer thickness of 2 µm. The dashed lines are a guide to the eye.

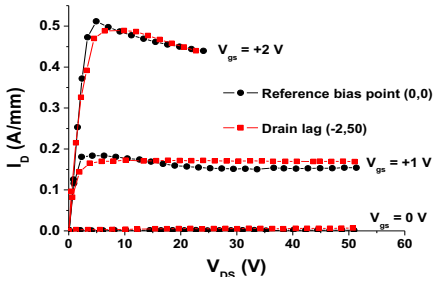

Figure 6: Transfer characteristics and pulsed IV measurements

Thanks to proper optimisation of the GaN buffer, as well as of the top passivation (combination of in-situ and ex-situ passivation), the devices characteristics measured in different pulsed conditions do not vary, as would occur in case of traps effect. Figure 6 show the pulse IV characteristics of an e-mode device, based on a ultra-thin AlN barrier.

IV. Switching Characteristics

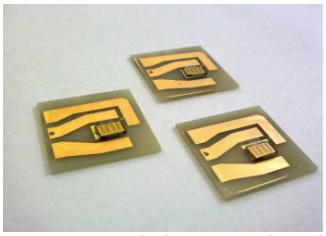

Figure 7: Power DHFET devices mounted on AlN ceramic for measurement purpose

We have also studied the switching device characteristics. For that purpose, large power GaN-DHFETs were fabricated with a total gate width W_g = 57.6 mm.
The devices were mounted on an AlN ceramic substrate, as shown in Figure 7. A very small gate turn-on and turn-off of 32 and 44 ns

respectively were observed. Figure 8 shows the dynamic on-resistance (R_{dyn}) and gate charge values (Q_g) of the GaN transistor as they were measured using a boost converter setup. The dynamic on-resistance is around 0.23Ω and only shows a very minor increase with increasing off-state drain voltage ($V_{ds,off}$), proving the absence of the surface or bulk electron trapping in the device [7]. A total gate charge value of 10nC is obtained at $V_{ds,off}$=120V. These excellent properties result in low transistor losses (conduction respectively switching). It is clear that, due to the low Miller capacitance, a very fast switching behavior can be obtained: a first comparison shows that the GaN-DHFET can switch 5 times faster than a standard Si power MOSFET.

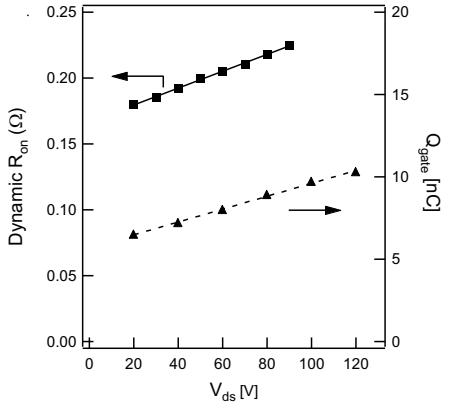

Figure 8: Dynamic on-resistance (R_{dyn}) and total gate charge (Q_g) of a GaN DHFET (W_g = 57.6mm), measured using a boost converter [7].

V. RELIABILITY ASPECTS

Finally, the reliability study of those components is also addressed. First storage tests are reported. A collection of 50 SiN/AlGaN/GaN HEMT (2x100µm) devices has been fully characterised and then stored at a temperature of 325ºC up to 1000 hours. The devices have been monitored both in DC and pulsed mode and results are reported in Fig. 9. We show that GaN-on-Si devices can withstand high temperatures without severe degradation of the forward current, nor the threshold voltage. After a slight burn-in visible after 24h, the dc characteristics stabilize and we don't see any modification of the pulsed IV curves (not shown here). The device leakage current slightly increases but remains well below specification.

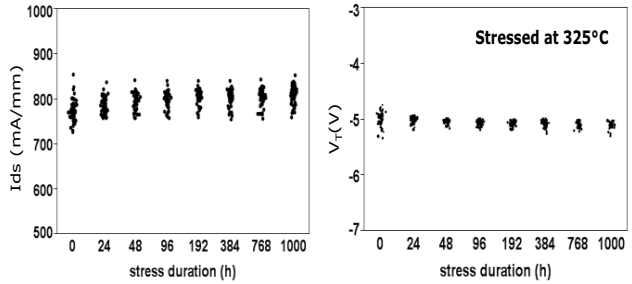

Figure 9 : Monitoring of 50 GaN-on-Si HEMTs (2×100 µm) during temperature stress at 325°C: Drain current density at V_{GS} = +1 V and V_{DS} = 50 V (left) and threshold voltage (right) up to 1000 hours.

Devices have also been studied at high temperature under stress, both in off-state and in on-state, as shown in Fig. 10. GaN-on-Si HEMTs, with gate-drain distance as small as 5 µm, can be stressed up to 200 hours in off-state at 200 V and 200°C [8]. In on-state, gate bias voltage has been applied to reach a junction temperature of 280°C. The devices have been stressed so far up to 120 hours. Sole a slight modification of the gate leakage current characteristic has been observed. All our devices are processed using a Schottky gate. The development of a gate dielectric would certainly be beneficial for switching devices.

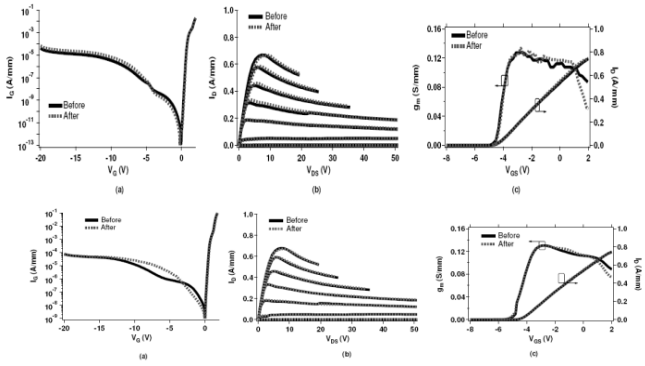

Figure 10: Comparison of the DC device characteristics of SiN/AlGaN/GAN HEMT devices before and after stress. Top: in on-state, at Vgs=+2V, Tj=280ºC after for 120 hours; Bottom: in off-state at Vds=200V, T=200 ºC after 360 hours.

CONCLUSIONS

GaN-on-Si depletion and enhancement-mode devices have been reported, benefiting from in-situ SiN passivation. SiN, by providing charges to the AlGaN surface, plays a key role in achieving good electrical device performance as well as offers an additional degree of freedom for device design engineering. Its impact on mechanical properties of the epilayer stack is further key for material stability, even at elevated temperatures.

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