Mobile Electrostatic Carrier (MEC) evaluation for a GaAs wafer backside manufacturing process

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ABSTRACT

Backside processing of GaAs wafer for MMIC applications is known as manual handling and processing of very thin wafers in the range of several mil. In common production flows the frontside finished wafer will be sticked on a sapphire carrier for backside processing using thermoplastics or wax by a temporary wafer bonding process. The sapphire carrier mechanically assists the wafer during the thinning, through wafer via etch and metallisation process modules. After the metallisation the thin GaAs wafer will be de attached from the sapphire carrier by a de bonding process. In order to reduce the manual thin wafer handling during the de bonding process module a mobile wafer carrier has been produced and tested. In this work we present a MEC (Mobile Electrostatic Carrier) for temporary bonding of thin GaAs wafers using electrostatic force for processing and handling in a wafer manufacturing area.

INTRODUCTION

The MEC is realized on a sapphire wafer using backside contacts for charging. The thermal expansion coefficient of sapphire is very well adjusted to the GaAs material. Figure 1 shows a schematic of the MEC. There are two electrodes on the front side of the MEC that are connected by TSV (Through Substrate Vias) to recessed contact pads at the back side of the sapphire carrier. The recessed contact pads avoid the discharge of the MEC, when it is put on conducting wafer chucks. On top of the electrodes E1 and E2 there is realized a dielectric stack that is enabling the separation of charges between the electrodes E1 and E2 and the afterwards clamped wafer that serve as opposite electrode.

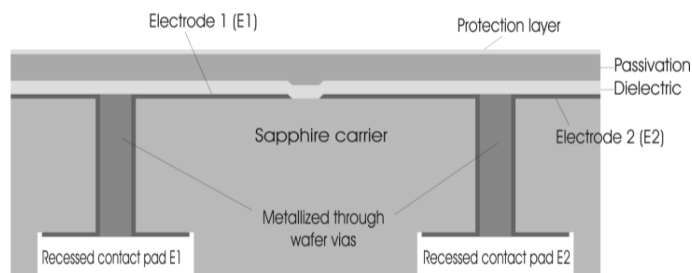
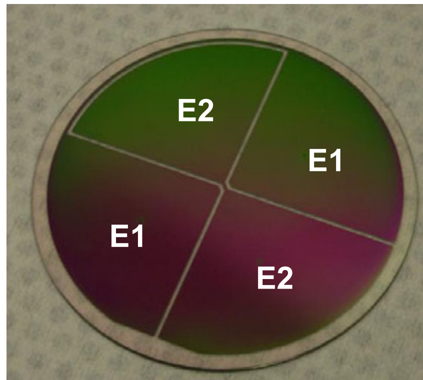


Fig. 1: schematic view of the MEC

The working principle is well explained in [1] and [2]. The thin wafer can be clamped by applying voltage between the contact pad E1 and E2. The thin wafer on the MEC has to be electrical conducting. Charges will be separated at the near surface of the wafer that builts up an electrostatic force for the wafer clamping.

Figure 2 shows a photograph of the front and backside of the MEC. In this configuration there exist four metal areas that are connected to a recessed contact pad at the back side. The opposite metal areas are connected together at the front side by metal lines. There are two electrodes with two TSV per electrode.



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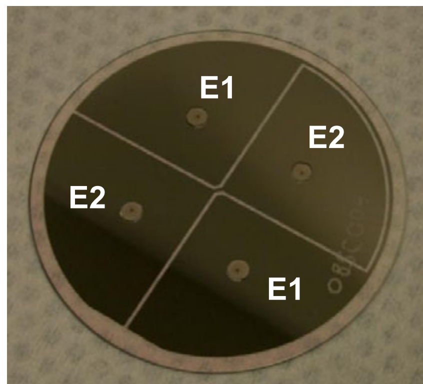
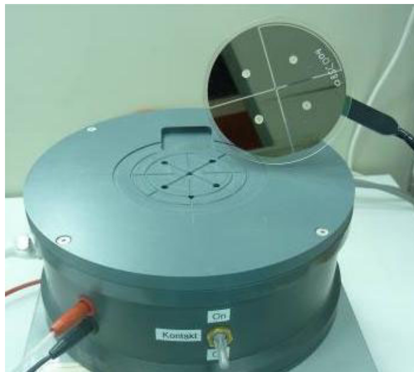


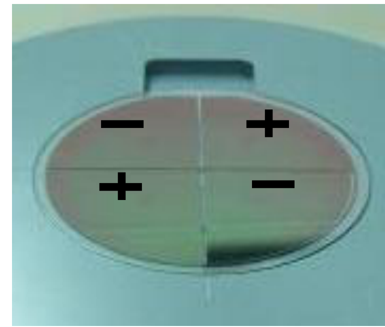
b)

Fig. 2: photograph of the mobile electrostatic carrier (MEC), a) front side, b) rear side of MEC

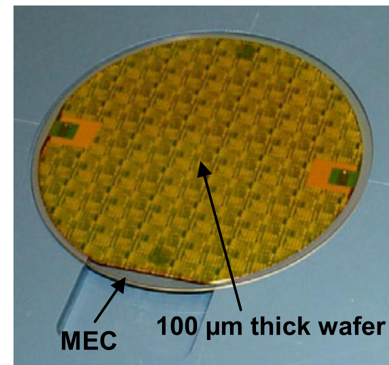
For the charging of the MEC there is used a charging station shown in figure 3. The MEC is put with the backside on the tool and it is clamped by vacuum then the pins will go up to the contact pads of the MEC and the voltage is applied for charging the MEC.



a)



(b)



(c)

Fig. 3 : charging station MEC (a); vacuum clamped MEC on tool with applied voltage (b); thin clamped wafer (c)

In order to clamp a thin wafer the MEC stacked with a thin wafer is put on the tool. After the clamping of the thin wafer the wafer can be processed by several semiconductor tools that encapsulate the four contact pads at the backside from fluent or gaseous electrical conducting media.

MEC CHARACTERISTICS

The main parameters are the leakage current and the electrical capacity that define the quality of the MEC. A low leakage current between the electrodes enables a long electrostatic clamping and a high electrical capacity provides a high bonding force. The used MEC shows a leakage current of about 0.2 nA which results in voltage drop from 200V to 120V in 34 hours at room temperature. The electrical capacity measured at 40V results in about 10.5 nF that corresponds to a theoretically bonding force of about 250N at an applied voltage of 200V for a 4 inch wafer. The bonding force at 120V is about 100N and is high enough to withstand the needs for the processes we tested. For the usage of the MEC in a semiconductor process the temperature stability of the leakage current is

very important. Figure 4 shows the increase of the leakage current vs temperature measured with and without a stacked silicon wafer. The leakage current of the MEC increases very strong above temperatures of 150°C, so the electrostatic clamping force will drop. It is concluded that the electrical insulation at the surface of the MEC yet isn't perfect. The problem might be related to the preparation of the TSV. The smoothness of the aperture of the via holes at the front side is of crucial relevance for the electrical insulation after deposition of dielectric films. These technological steps can be further improved. Leakage measurements performed without a stacked wafer on the MEC does not show such strong leakage current increase as shown in figure 4.

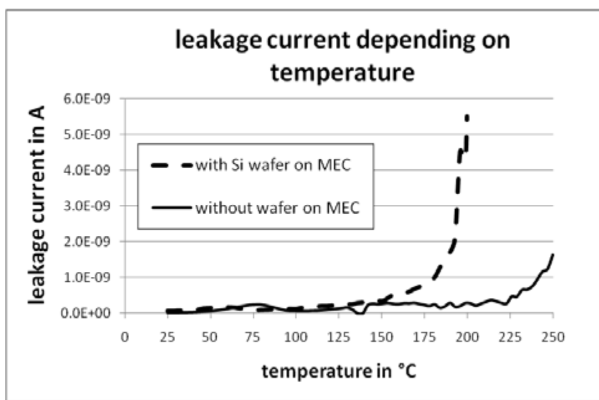


Fig. 4: leakage current of the MEC depending on temperature measured with stacked and without Si wafer

PROCESS EVALUATION

The backside process for MMIC applications on GaAs wafer processing consists of five process modules. These modules are the bonding of the front side processed wafer on a carrier, thinning of the wafer, through wafer via etching, the backside metallisation for the ground plate and the debonding of the thinned wafer. In this work the use of the MEC is focused on the de bonding process module. It consists of the slice off of the thin wafer that is attached to the sapphire carrier using thermoplastic bonding adhesive. Afterwards the remaining bonding adhesive on the wafer surface has to be removed by a wet and dry chemical process. The wet chemical process removes the main thermoplastic material. After the solvent rinse an oxygen plasma is applied that removes veils and organic residues. After the cleaning it follows the electrical and optical wafer inspection steps. Figure 5 shows a process flow that is tested in this work. All steps described above are performed using the MEC for the thin wafer processing and handling. During de bonding on a hot plate 5(B) in preliminary tests there arise problems with the clamping force of the wafer stack on the MEC. As described above the leakage current is still too high at temperatures above 150°C. The de bonding does not work correctly during the tests because of the high leakage at 200°C de bonding temperature. Furthermore if the bonded wafer on saphirre or MEC show a bow greater than 10 µm the clamping of the wafer pair on the MEC does not work correctly because of a too big air gap between the MEC and the wafer. It reduces the electrical capacity and thus the clamping force. In order to avoid this problem the bow and leakage currents have to be improved at high temperature. However the clamping of the de bonded thin wafer works excellent. The thin wafer shows no stiffness like the bonded wafer pair and it adapts very well to the MEC with high clamping force.

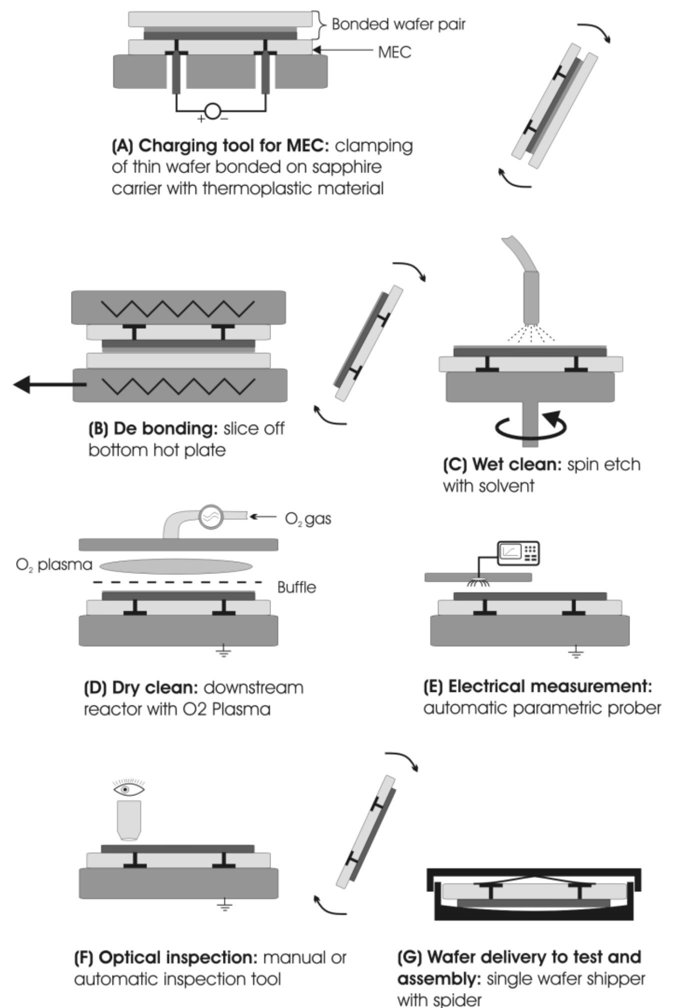


Fig. 5: process flow of de bonding module using the MEC

Therefore the work continued with the wet cleaning 5(C) on a manual spinning tool. Figure 6 shows a coater that is

used for the preliminary tests in order to perform the wet chemical clean. The wafer is cleaned after dispensing 20 ml solvent over 30 s at a spinning speed of about 1000 rpm. After the solvent rinse for the thermoplastic material removal the wafer drying is done using a rinse with IPA over 10 s at a speed of 5000 rpm plus 5 s drying. For the dry chemical cleaning 5(D) there is used a downstream plasma tool with an automatic wafer handling system. Tests on the tool show that the MEC is discharged by the wafer chuck during the O2 plasma clean. It is assumed that the root cause is the ignition of a parasitic plasma burning in the recessed contacts of the MEC. This plasma discharges the carrier with the contact of the plasma and the conductive wafer chuck. Tests performed at a dry etching tool show no discharging with an isolated wafer chuck.

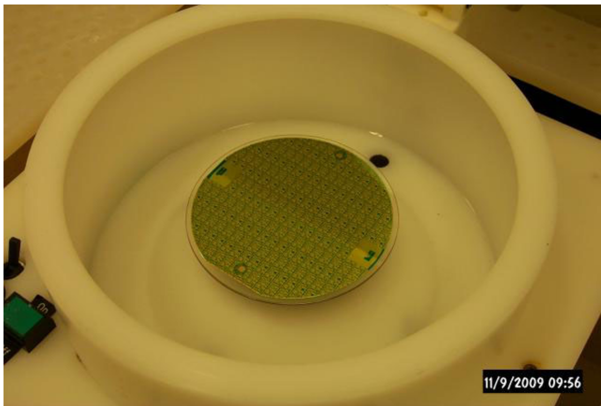


Fig. 6 : wet chemistry spinning tool with thin wafer clamped by the MEC

In addition measurements of DC data on PCM (Process Control Monitor) transistors are done on an automatic testing tool 5(E). Major focus on the testing was the electrostatic principle affecting the measurement or not. Additionally effects are suppressed by doing measurements with an electrostatic carrier and a perforated sapphire carrier with vacuum clamping. A DC output and input characteristic curve is measured on a manual test bench shown in figure 7. The curves with and without the MEC are looking quite similar. The transconductance G_m and drain current I_{ds} are not influenced by effects from electrostatic fields of the MEC. The metal plate on the back side of the chip shields the transistor from the electrical fields and this means there will be no back gating effects possible.

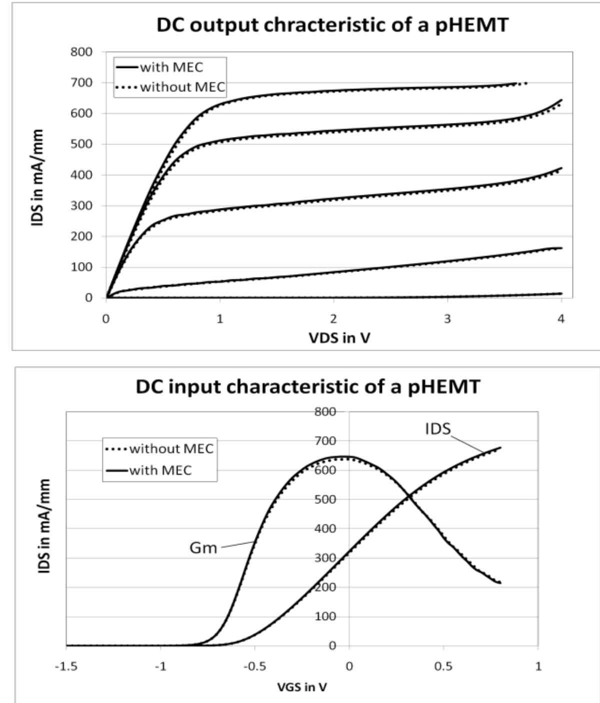


Fig. 7: DC characteristic curves of a pHEMT transistor with single gate finger width of 100µm

The parametric PCM test is performed on an automatic testing tool with a cassette loading station and flat alignment as shown in figure 8.

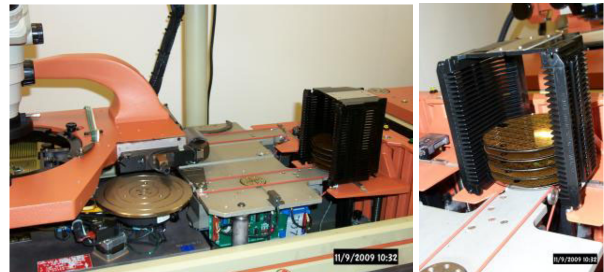


Fig. 8: automatic testing tool for PCM paramtric measurements

On this tool the active and passive devices of the PCM that represents the devices of the integrated circuits are measured. The Idss saturation current that is measured at 0V V_{GS} and 2V V_{DS} shows the same distribution of the currents with and without the support of the MEC shown on the mappings in figure 9.

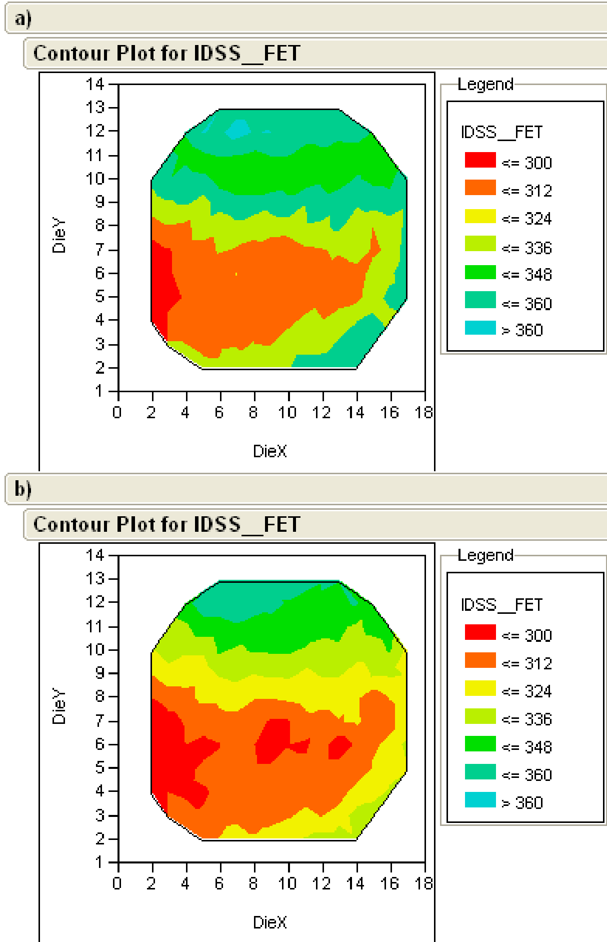


Fig.9: Idss (mA/mm) mapping of 4 inch wafer at PCM Test level (163 sites measured) without (a) and with (b) MEC

Additionally the contact resistance of the source vias is measured without any problems and it enables the electrical test controling the backside process (figure 10). The mean value is about 9.8 mOhm for both resistance measurements with an equal distribution. After than the optical inspection 5(F) is possible either manually or on an automatic inspection tool before it will be used as transport carrier for delivery 5(G) of the thin wafer in a single wafer shipper box. Up to now there is reached a secure clamping time of 34 hours. If the leakage current can be further reduced the shipping of wafers will be more reliable.

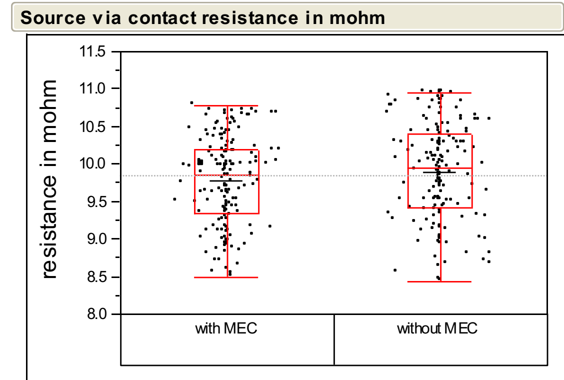


Fig. 10: Source via contact resistance measured on 163 sites on the wafer with and without MEC

CONCLUSIONS

The work illustrates a backside process module for a GaAs manufacturing process with the support of a mobile electrostatic carrier. Process tests are evaluated on different tools and a possible influence of the MEC on the process results are characterized. The thin wafer clamped on the MEC shows a secure automatic and manual handling on the tools and allows optical flat alignment. Further investigations are necessary in order to reduce the leakage current vs temperature of the MEC. This process is applied on a small quantity of engineering wafers with reproducible results without wafer breakage.

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