Low RF power SiC Substrate Via Etch

Ju-Ai Ruan, Sam Roadman, Wade Skelton

TriQuint Semiconductor, 500 W Renner Road, Richardson, TX 75080-1324
Phone: (972) 994-3842, e-mail: jruan@tqs.com

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Abstract

Effect of coil RF power on pillar formation in SiC via etch using ICP etching process has been studied. It was observed that when using only a typical etching chemistry such as SF_6 in the reactant and as coil RF power is reduced to certain threshold, pillar density starts to increase drastically. By properly modifying the etching process especially the reactant mixture, it is possible to obtain pillar free result at substantially reduce coil RF power. This selection of parameter space enables the wafer to stay at relatively low temperature during SiC via etch. This opens up new alternatives to simplify the backside process.

INTRODUCTION

As a wide band gap semiconductor material with high thermal conductivity and high temperature stability, silicon carbide (SiC) is widely used for high power MMIC applications. SiC is also used as a substrate for epitaxial growth of GaN for even higher power MMIC devices [1]. In both cases, electric connection is often made through the backside of the device (through backside via) to further improve device performance. Thus for the fabrication of SiC based devices, either devices built directly on SiC, or GaN devices using SiC as substrate, backside SiC via etch is an essential part of device fabrication.

Many previous studies emphasized a desirable high SiC etch rate and high etch selectivity to etch mask materials. In our recent study, an etch rate of ~ 1um/min and SiC to GaN etch selectivity >25 were obtained using SF_6 etch chemistry and an ICP etching platform [2]. In that study, aspects related to process sustainability, especially on pillar reduction was also discussed. It was noted that under prolonged chamber operation, and if the chamber is used to etch both SiC and GaN, pillar formation is often an issue affecting process sustainability. Proper seasoning after GaN etch or after the chamber subjected to a wet clean can generally reduce pillar formation. Pre-etch wafer clean can also have substantial effect on pillar formation.

In the same study [2], it was observed that while SiC etch rate varies relatively slowly with coil RF power, pillar formation can dramatically increase as coil RF power is reduced to below certain threshold. This phenomenon also existed and was reported for some other etch processes. For example, Westerman et al. [3] mentioned that for GaAs via etch, pillar formation can be reduced through the use of higher ICP power, higher Cl2 flow and lower process pressure. These results seem to indicate a general trend of ICP power on pillar formation, with higher ICP power generates less or no pillar formation. For this reason, coil RF power is typically kept at relatively high level to ensure pillar free etching.

An unintended consequence of etching SiC at high coil RF power is that wafer can become very hot during etch. This imposes certain restriction on the back end process integration. For example, in a typical backside via formation process, wafers are generally mounted onto carrier substrates using adhesives, with the device side facing the carrier substrates. The backside of the wafers are ground to proper thickness (typically around 100 um). Vias are patterned using a hard mask. The wafers are then etched to form backside via. After via etch and subsequent metallization, the wafers are separated from their carrier substrates.

Since during via etch, wafers are heated up by ICP RF power, the adhesives used to bond the wafers to their carrier substrates must be able to sustain sufficiently high temperature to avoid adhesive melt. Epoxy is often used as the bonding material since its bonding strength only starts to degrade at temperatures above 177 ^{0}C [4]. Yet epoxy must be chemically dissolved in order to separate the wafers from their substrate. This separation process can be quite cumbersome and lengthy. If low temperature adhesives such as wax can be used, it would be much easier to separate the wafers from their carrier substrates. The use of low temperature adhesives in turn requires a via etching process to be performed at relatively low temperature. For this purpose, minimizing the RF power during ICP etch would be desirable. Yet as mentioned previously, pillars tend to form at reduced RF power. Eliminating pillar formation at reduced RF power is thus useful.

In this paper we report the result of our recent study that demonstrates a new SiC via etch process at much reduced RF power with pillar free result. Under the new process condition, wax can be used as the adhesive to bond the wafers to their carrier substrates without causing localized wax melt.

EXPERIMENT

Inductively coupled plasma (ICP) etch tool with optimized ICP source was used for the experiments. For pillar formation studies, SiC samples were first ground to remove about 10 um of SiC, then polished to remove another 1 um of SiC. Samples were patterned to form via pattern (~60 um via diameter) with Ni as the etch hard mask. Sample was cut into small pieces (~1cm x 1cm in size) and mounted onto Ni-plated sapphire carrier wafers. Etch was first conducted at various coil RF power at fixed platen bias to observe the effect of coil RF power on pillar formation. Additional tests were conducted at fixed low coil RF power, but process pressure, reactant chemistry and flow rates were varied to obtain pillar free etching result. In all cases, samples were sputter cleaned prior to etch to remove any residue and potential grind damage left on SiC surface. After a pillar free etching result has been obtained at the low coil RF power at certain process pressure, reactant chemistry and flow rates, the pressure and reactant chemistry and flow rates were fixed at their respective settings and the coil RF power was further reduced to test pillar free process margin vs. coil RF power under the new condition.

Etch rate and SiC to GaN selectivity studies were also performed. SiC samples were 6H n-type SiC. GaN samples were GaN grown on SiC. A piece of each of these two samples (also about ~1cm x 1cm) was mounted onto a Ni-plated sapphire substrate and was partially covered with Kapton tape to leave an un-etched reference region. Etch was conducted on all two samples at the same time. The mask tape was removed and sample surface was cleaned after etch. Step heights between etched and un-etched regions were measured using a profilometer. Etch was conducted at a fixed low coil RF power, and under various platen bias, process pressure, and reactant flow rate. The variation of the process parameters is limited in the range where pillars do not occur.

RESULT

PILLAR FORMATION VS. RF POWER

Etching test was first performed at high coil RF power under what is known as BKM (best known method) process. No pillar formation in this etching condition, Figure 1(a). The coil RF power was then reduced in subsequent tests (but for each test coil power was fixed). At low coil RF power (45% of BKM setting), substantial amount of pillar formation occurred, Figure 1(b). Under further reduced coil RF power condition (32% of BKM setting), via etch was completely impeded, Figures 1(c) and 1(d), where Figure 1(d) is a magnified section of the via shown in Figure 1(c).

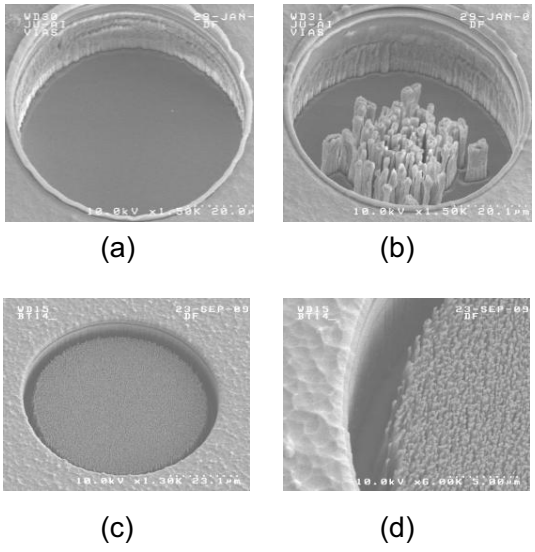

Fig 1 Typical SEM image of via etched at (a) high coil power; (b) at low coil power, and (c) further lower coil power. Fig (d) is a magnified section of (c)

In order to obtain pillar free result at low coil RF power condition, other process parameters including pressure, reactant composition and flow rate were optimized. We found that changing reactant composition had the most amount of impact on pillar formation. Under certain combined conditions of pressure, reactant composition and reactant flow rates, pillar free result was obtained at even further reduced coil RF power condition. This is show in Figure 2, which is the SEM image of a via etched at 28% of the BKM coil RF power.

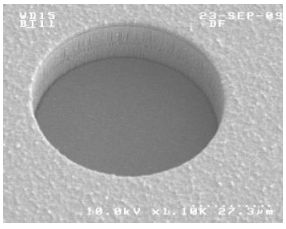

Fig 2 Typical SEM image of via etched at 28% of BKM coil RF power but under optimized process pressure, reactant composition and flow rates.

ETCH RATE AND ETCH SELECTIVITY

Not only pillar formation is sensitive to coil RF power, etch rate and etch selectivity also are a function of coil RF power. At reduced coil RF power, etch rate was generally reduced. However, the etch rate reduction is not proportional to the reduction of coil RF power. For example, when coil RF

power is reduced by 50% from BKM setting, etch rate is reduced from ~ 1um/min to 0.8 um/min. But this etch rate is still high enough to be of manufacture worthy.

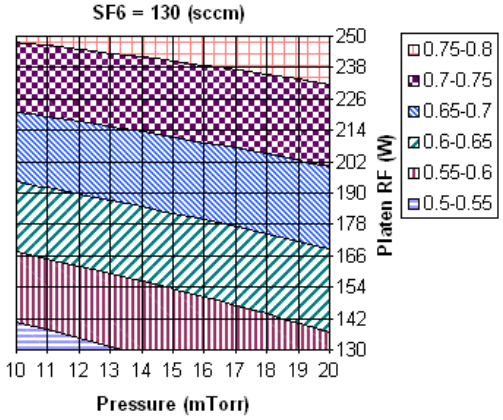

Fig 3 Contour plot of etch rate vs. pressure and platen RF power at fixed SF_6 flow rate and low coil RF power.

Over all, etch rate is strongly dependent on platen RF power, as shown in Figs 3 and 4, where Fig 3 is a contour plot of etch rate as a function of process pressure and platen RF power at fixed SF_6 flow rate (130 sccm), and Fig. 3 is a contour plot of etch rate as a function of platen RF power and SF_6 flow rate at fixed process pressure (10 mTorr), both figures are for low coil RF power. It can be seen that in both cases, etch rate varies rapidly with platen RF power but varies relatively slowly with either pressure or SF_6 flow rate.

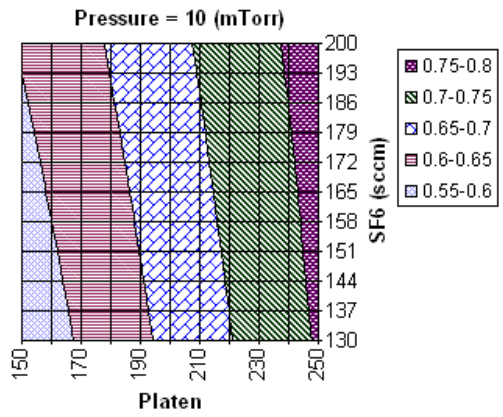

Fig 4 Contour plot of etch rate vs. SF_6 flow rate and platen RF power at fixed process pressure and low coil RF power.

At fixed platen RF power, etch rate variation dependents on both pressure and SF_6 flow rate to the same degree, as shown in Fig 5. Increasing pressure or SF_6 flow rate increases SiC etch rate.

SiC to GaN etch selectivity (SiC:GaN etch ratio), on the other hand, displays a more complex relationship to pressure and SF_6 flow rate. This is shown in Fig. 6. The range of etch selectivity in this figure is from 18 to 22.5 (i.e., SiC:GaN etch ratio from 18:1 to 22.5:1). This is adequate for most practical application. Etch selectivity decreases with increased platen RF power, not shown.

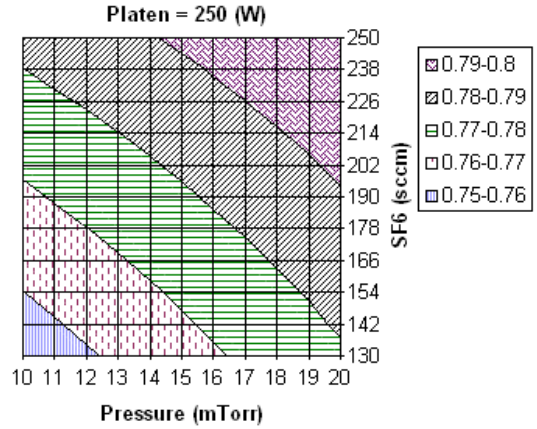

Fig 5 Contour plot of etch rate vs. SF_6 flow rate and pressure at fixed RF power.

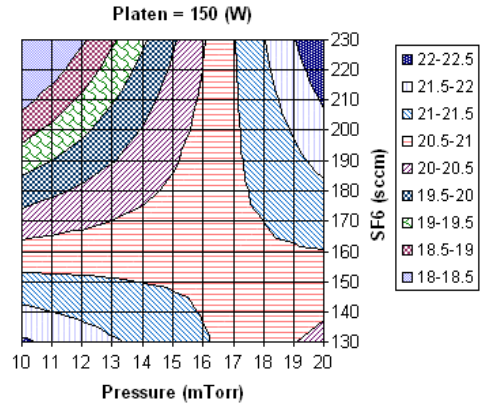

Fig 6 Contour plot of SiC to GaN etch selectivity vs. SF_6 flow rate and pressure at fixed RF power.

We estimate that wafer temperature at low coil RF power condition is less than 80 ^{0}C in our test. This is concluded based on the post etch appearance of low temperature adhesives (used to bond the test samples to their carrier wafers). If sample temperature exceeds 80 ^{0}C as is the case under high coil RF power, the adhesive clearly melts and often leaves small voids behind after the samples cool down. But there is no sign of the adhesives got melt during etch. Demounting process can be substantially simplified as a result.

CONCLUSION

Within a large range of coil RF power, SiC etch rate decreases slowly with the decrease of coil RF power. However, etch rate increases with the increase of platen RF power rapidly. SiC to GaN etch selectivity increases with coil RF power but decreases with platen power. Pillar formation is generally reduced at high coil RF power and becomes a real issue when coil RF power is reduced to certain threshold when using only a typical etching chemistry such as SF_6 in the reactant. However, with modified reactant mixture and flow rate, it is shown that coil RF power can be significantly reduced and still obtaining pillar free results. The modified etching process allows the use of low temperature adhesives to substantially simplify the via formation process.

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ACRONYMS

ICP: Inductively coupled Plasma