Stress Suppression of Backside Metal in GaAs Devices

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Abstract

In a Ni-P/Au electroless plating backside electrode, the stress of a thin Ni –P film induced by annealing has been investigated using Stress gage, AES depth profile, X-ray diffraction measurements. Over around 100ºC temperature annealing, Ni diffusion was observed and the stress increased. With Ni diffusion, the Ni-P layer changed to P rich composition and to crystal from amorphous. The stress was caused by the crystallized Ni-P layer and the Ni diffusion layer. The increase of the stress is effectively suppressed by inserting the Pd barrier metal under Ni-P.

The Pd/Ni-P/Au backside electrode makes it possible to form highly uniform and highly thermally stable metallization through via-hole on GaAs substrate.

INTRODUCTION

As for backside electrodes in GaAs devices, Au plating film is used. As a seed layer, the sputtering or evaporation coating such as a Ti/Au thin film is generally used. The improvement of the coverage for the seed layer through a via-hole is still required. We found that Ni-P electroless plating can be used as a seed layer of Au plating with uniform coverage through via-holes.

The stress of the Ni-P electroless plating film increases up to 800-1000MPa after annealing, while the stress of the conventional evaporation or sputtering coating is almost stable. This results in the large bow of GaAs wafers up to 5 mm at 0.5μm Ni-P film on 4-inch thin GaAs substrate. Wafer bow causes fatal troubles of a handling, a wafer clack, a chucking error of the wafer test.

In this work, we discuss the origin of the stress increase of the Ni-P electroless plating film and also demonstrate the suppression of the stress increase after annealing by employing a Pd barrier layer under the Ni-P film.

1. NI-P THIN FILM ON GAAS SUBSTRATE

Polished 4-inch (100) GaAs wafers with 625 μm thickness were used. The Ni-P electroless plating films with thickness between 0.29-0.30μm are formed on the GaAs wafers. After annealing, the Ni-P layer showed tensile stress. Figure 1 shows the annealing temperature dependence of the stress of Ni-P, which was calculated from the wafer bow. Annealing time is each 4 hours. The steep increase is observed by five times after annealing over around 150ºC. Figure 2 shows the SEM image of the samples before and after annealing. The Ni diffusion layer is formed between layers of Ni-P and GaAs. This layer is a metastable phase, Ni_2GaAs formed on (001) GaAs annealing at 100ºC-300ºC[1]. Figure 3 shows the Ni-P and Ni_2GaAs layer thickness variation as a function of annealing temperature in each temperature. The Ni-P layer thickness decreased and Ni_2GaAs increased by the annealing of over around 100ºC. The change of the thickness of both layers was saturated over 150ºC. From this result, the stress increase might be closely related to the Ni diffusion.

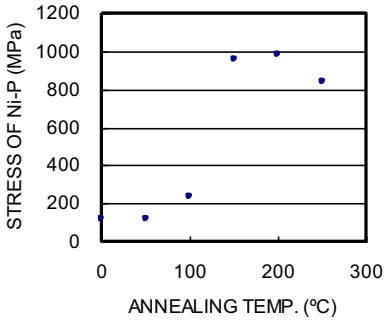


Fig. 1. Annealing temperature dependence of the stress of Ni-P layer

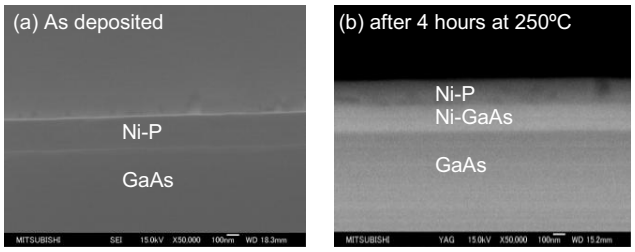


Fig. 2. SEM image of vertical cross section of As-Deposited Ni-P on GaAs and after annealing for 4 hour at 250ºC

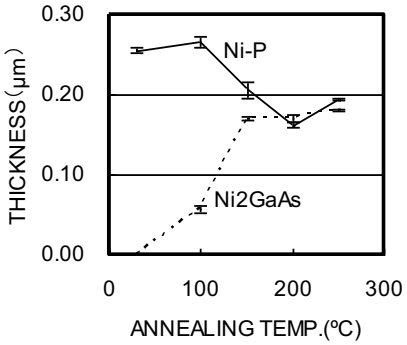


Fig. 3. Annealing temperature dependence of Ni-P, Ni_2GaAs thickness

2. Evaluation of each stress in Ni-P layer and Ni_2GaAs layer

In order to estimate the each layer stress of Ni-P and Ni_2GaAs after annealing for 4 hours at 250 ºC, the Ni-P is removed by ion milling and measured the wafer bow of remaining Ni_2GaAs on GaAs substrate, and finally the stress calculated from the wafer bow.

The stress of a thin layer on the wafer is estimated from the wafer bow. The stress is given as follows[2]:

$$\sigma = \frac{E_s t_s^{\,2}}{6(1-\nu_s)Rt_F} \quad \text{-------- (1)}$$

E_s, ν_s, t_s, t_F, R are a Young's modulus, a Poisson's ratio, the thickness of the substrate, the thickness of the film, the curvature radius, and the stress of the film, respectively.

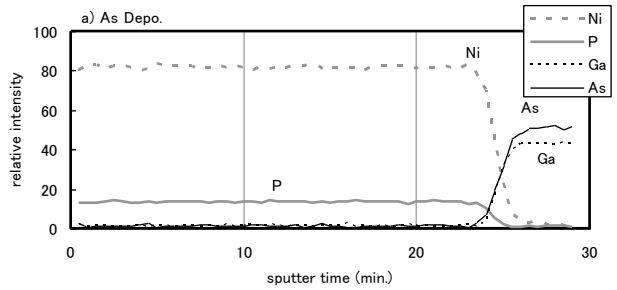
Table I shows the film thickness and the wafer bow and the stress. The stress of Ni_2GaAs single layer is 440MPa. The wafer bow caused by removed Ni-P layer is 11.99μm. The stress of removed Ni-P is 660MPa, given from the equation (1).

TABLE I
FILM STRUCTURE AND WAFER BOW AND STRESS

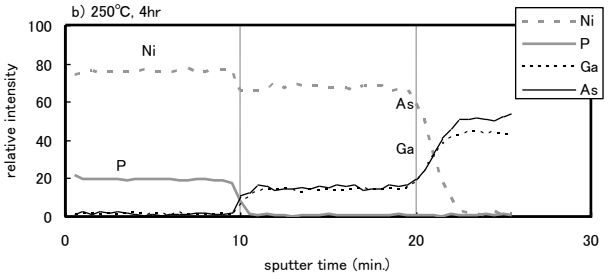
	Thickness		Wafer Bow	Stress
	Ni-P	Ni_2GaAs		
As-Depo	0.27μm	-	5.55μm	130 MPa
250ºC/4hr	0.17μm	0.16μm	28.08μm	-
After Ion Milling	-	0.15μm	16.09μm	440 MPa

3. Origin of stress increase afeter annealing

We analyzed AES depth profiles and XRD patterns of the samples before and after annealing for 4 hours at 250ºC , to study the origin of stress increase. Figure 4 and 5 show AES profiles and XRD patterns, respectively. The AES measurements were performed using a primary beam of 10 keV with Ar ion sputtering for compositional depth profile. The XRD was performed using CuKα radiation. Figure 4 shows that the composition of the Ni-P films changes to P rich phase and the growth of the Ni_2GaAs diffusion layer after annealing. It is reported that Ni_2GaAs forms an epitaxial crystal on the surface of the GaAs substrate[1]. XRD patterns indicate clearly change from a broad peak to some sharp peaks. This reveals the phase transition from amorphous to crystal after annealing. P rich shift in the composition of the Ni-P film may be well correlated with the crystallization of the film. It is suggested that the crystallization of the film may increase the stress of it. We think that the increase of the stress in the Ni-P film on GaAs after annealing is the growth of the Ni diffusion layer and crystallization of the film, originated from the Ni diffusion.

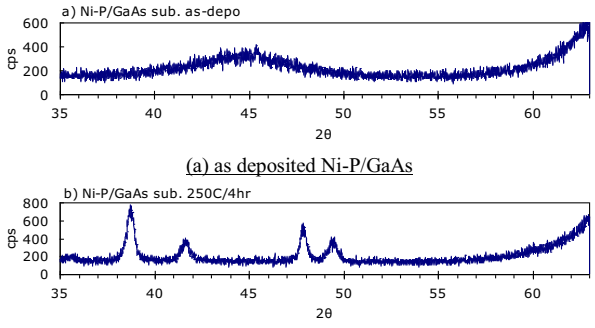


(a) as deposited Ni-P on GaAs



(b) After annealing for 4 hours at 250ºC

Fig. 4. AES depth profiles of (a) as deposited. Ni-P on GaAs sub and (b) after annealing for 4 hour at 250ºC



(a) as deposited Ni-P/GaAs

(b) After annealing for 4 hour at 250ºC

Fig. 5. XRD patterns of (a) as deposited Ni-P/GaAs, and (b) after annealing for 4 hour at 250ºC

4. Suppression of Stress of Ni-P film

We tried to decrease the stress of the Ni-P film on GaAs substrate after annealing by suppressing the Ni diffusion

after annealing. The Pd film is employed under the Ni-P film as a barrier metal for Ni diffusion, because the Pd films is easily electroless plated on GaAs and respected the similar barrier effect as a Pt film.

In table II, we shows the stress and the wafer bow of samples annealing at 250ºC for 4 hours. The sample with the Pd barrier layer suppressed the wafer bow effectively. Figure 6 shows XRD profile of Ni-P/Pd/GaAs sample. There is a broad peak of Ni-P amorphous which indicates that the Ni-P film is not crystallized. Some other sharp peaks show Pd-Ga-As compounds[3, 4].

TABLE II
LAYERS STRUCTURE DEPENDENCE OF WAFER BOW

	Thickness(as-depo)		After annealing at 250ºC	
	Barrier	**Ni-P**	**Stress of Ni-P**	**Wafer bow**
Ni-P/GaAs	-	0.27μm	891.6 MPa*	23.34μm
Ni-P/Pd/GaAs	0.10μm	0.30μm	407.6 MPa	17.12μm

*Average stress of Ni-P and Ni_2GaAs layer

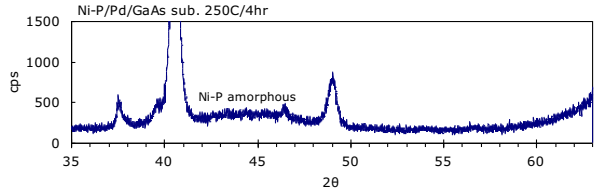


Fig. 6. XRD patterns of Ni-P/Pd/GaAs after annealing for 4 hour at 250ºC

CONCLUSIONS

In a Ni-P/Au electroless plating backside electrode, we found that the increase of the stress in the Ni-P film on GaAs after anneal is the growth of the Ni diffusion layer and crystallization of the Ni-P film, originated from the Ni diffusion.

We successfully suppressed the stress of the Ni-P film with inserting a Pd barrier layer between Ni-P and GaAs substrate. The Ni-P/Pd/Au backside electrode plate makes it possible to form highly uniform and highly thermally stable metallization through via-hole on GaAs substrate.

REFERENCES

[1] A. Lahav, N. Eizengerg, and Y. Comem, J. Appl. Phys., Vol.60, No.3, (1986).
[2] H. Yamadera, R&D Review of Toyota CRDL, Vol.34, No.1, (1999).
[3] J. O. Olowolafe, J. Appl. Phys., Vol.50, No.2, (1979).
[4] T. S. Kuan, J. L. Freeouf, P. E. Batson, and E. L. Wilkie, J. Appl. Phys., Vol.58, No.4, (1985).

ACRONYMS

XRD: x-ray diffraction
AES: Auger Electron Spectroscopy
SEM: Scanning Electron Microscope