Failure Investigations on AlGaN/GaN HEMTs for Different Sheet Resistances by Means of Raman Thermography

Helmut Jung[a], Michael Hosch[b], Reza Behtash[a], James R. Thorpe[a], Franck Bourgeois[a], Stefanie Held[a], Hervé Blanck[a], Andrei Sarua[c], Nicole Killat[c], Martin Kuball[c], and Thomas Roedle[d]

[a] *United Monolithic Semiconductors GmbH, Wilhelm-Runge-Straße 11, 89081 Ulm, Germany*
[b] *Institute of Electron Devices and Circuits, Ulm University, Albert-Einstein-Allee 45, 89081 Ulm, Germany*
[c] *H.H. Wills Physics Laboratory, University of Bristol, Bristol BS8 1TL, United Kingdom.*
[d] *NXP Semiconductors, Gerstweg 2, 6534 AE Nijmegen, The Netherlands*

Helmut.Jung@UMS-Ulm.de, Phone: +49 7315053090

Keywords: AlGaN/GaN HEMTs, power devices, thermal management, reliability

Abstract

Blow up investigations on GaN HEMTs were performed. It is shown that the blow up power and the related device temperature limit depends on applied source-drain voltages and the sheet resistance of the 2DEG in the device.

INTRODUCTION

In recent years, the AlGaN-GaN HEMT technology has received increasing attention due to its excellent potential for high power applications. High RF power implies high current and high voltage capability. Both are provided by the superior AlGaN/GaN material properties. Owing to recent tremendous technological improvements record power densities up to 40W/mm have been reported [1]. In parallel with generating an increasing output power, also an increasing heat is generated during device operation. In addition to high device temperatures, there are also large E-fields, which both can have strong impact on device reliability [2, 3]. In this work we demonstrate for the first time that the blow up power on GaN HEMTs is directly related to the 2DEG sheet resistance of the epitaxial layer.

EXPERIMENTAL DETAILS

GaN-HEMTs were fabricated from an AlGaN/GaN epi structure, with standard ohmic and gate contacts, with sheet resistances ranging from 420 and 650Ω/sq. 0.5 µm Γ- gates were fabricated using a SiN hard masking approach and the transistor is then passivated with SiN. The wafers were placed on a vacuum heat chuck keeping base temperature constant at 25°C. Temperature analysis was performed on 8×400, 6x400 and 2x400 µm transistors (on wafer) by Raman thermography [4]. Power was increased continuously up to the point of catastrophic device failure, and temperature was traced as function of power, by increasing the current via the gate voltage at fixed source-drain voltages (V_{DS}) of 25V and 50V.

RESULTS AND DISCUSSION

Figure 1 shows the measured temperature as function of power density for a 8x400µm device on wafer with R_{sheet} = 440 Ω/sq at source-drain bias of 50V and 25V.

For 50V bias, device temperature was 250°C at a power density of 8.5 W/mm where the transistors typically underwent catastrophic failure. This limit was observed systematically on several transistors. Typically, near device failure, the gate current increased up to 20 mA, also shown in Fig. 1.

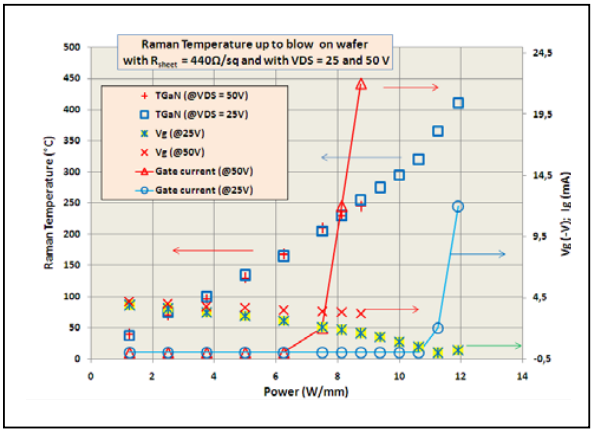

FIGURE 1: T-increase of a 8x400 µm transistor from wafer with R_{sheet} of 440 Ω/sq as a function of power density, biased with 25 and 50 V source-drain voltage until blown up. Applied gate voltages and the gate current near the blow up region are given in the figure, too.

For a corresponding test, performed at a source-drain voltage of 25V the transistors did not fail until much higher power levels (12W/mm) and higher temperatures (T = 420°C). Gate leakage also here increased drama-tically near the point of catastrophic failure.

Further experiments were performed on wafer with higher R_{sheet} (500 Ω/sq). In this case much higher power levels (12.5 W/mm) could be achieved even at V_{DS} = 50V, and devices also reached higher maximum temperatures of 470°C (Fig. 2). Gate current prior to catastrophic failure behaved similarly as for the previous devices.

The same trend was observed for a variety of wafers with different sheet resistances (Fig. 3), all having a similar layer structure. Additionally, transistors with different geometry (number of fingers and gate pitch) were tested yielding different temperature rise in the device at same power density.

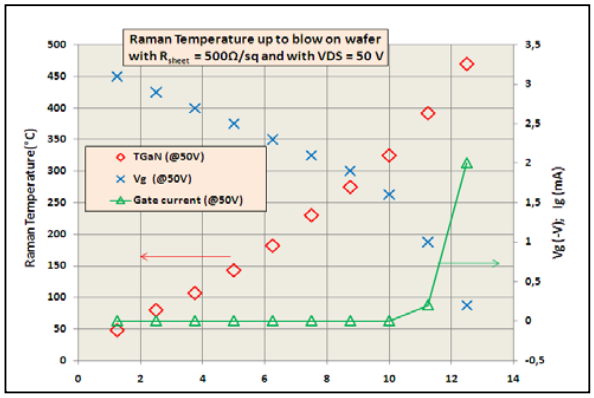

FIGURE 2: T-increase of an 8x400 µm transistor from wafer with R_{sheet} of 500 Ω/sq as a function of power density, biased with 50V source-drain voltage until blown up. Applied gate voltages and the gate current near the blow up region are given in the figure, too.

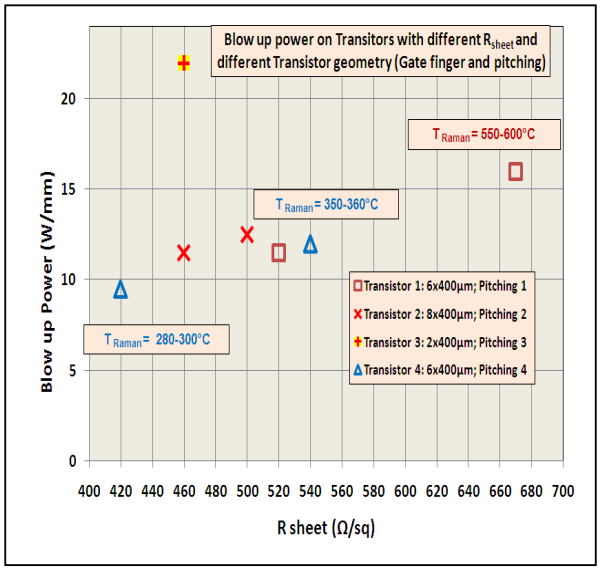

FIGURE 3: Blow up power limits as a function of sheet resistance for different device geometries. Corresponding measured by Raman device temperature *a*t blow up is also given alongside.

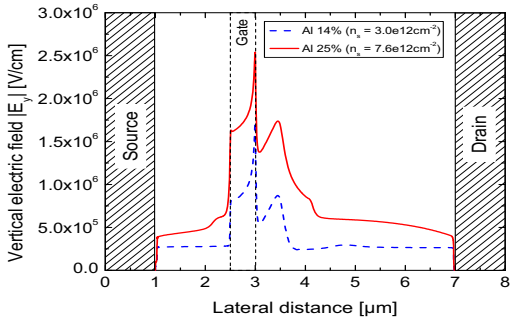

FIGURE 4: Vertical electric field distribution between source and drain in the AlGaN barrier of two AlGaN/GaN epi structures with different Al-content in barrier providing different R_{sheet} for V_{DS} = 50 V and P_{diss} = 2.8 W/mm.

The key result is a consistent trend of the higher the sheet resistance the higher the power limit for catastrophic failure in the investigated devices. Obviously temperature rise observed before blow up has also increased.

Figure 4 shows the magnitude of the vertical electric-field component in the AlGaN barrier determined from two-dimensional device simulations for two different wafers with Al-content of 14 and 25%, resulting in sheet carrier concentrations of $3x10^{12}$ cm^{-2} and $7.6x10^{12}cm^{-2}$, respectively for V_{DS} = 50 V and P_{diss} = 2.8W/mm. Wafers with higher carrier concentrations, e.g. lower 2DEG R_{sheet} exhibit significantly higher E-fields in the AlGaN-barrier, also to higher fields in the channel.

The blow up limit (power at catastrophic device failure) is a function of

(**i**) ***the local temperature*** and

(ii) the local maximum electric field, *which depends on* ***(iii) 2DEG sheet carrier concentration.***

The results suggest that in the case of the lower sheet resistance devices studied here high peak E-fields and related failure mechanisms may be a primarily responsible factor for the blow up observed limiting power handling of the transistor especially at high voltages (>25V), while for devices with higher sheet resistances, blow up power limit was less dependent on the applied voltage, suggesting that temperature here plays a significant role in device failure.

This new finding that the blow up power limit is de-pendent on sheet resistance is of fundamental importance for designing and biasing the GaN-transistors especially in the case of power devices.

CONCLUSIONS

Blow up investigations on GaN HEMTs were per-formed by means of Raman thermography. The power blow up limit was shown to be directly correlated with the 2DEG sheet resistance of the epitaxial wafer. The obser-vation that higher voltages and lower sheet resistances leads to lower blow up power of the transistors was ex-plained by a combination of critical local temperature and critical local maximum electric filed.

ACKNOWLEDGEMENTS

The authors would like to thank its cooperation partner from IAF, Freiburg or very constructive discussions and support through the PhiluGaN Project.

REFERENCES

[1] Y.-F. Wu et al. 40W/mm Double Field-Plate GaN HEMTs, IEEE DRC 2007, June 2007

[2] Jimenez et al, Reliability Physics Symposium, 2008, IRPS 2008.

[3] Meneghesso et al. Light emission in GaN HEMTs: IWN2009 Montreux

[4] A. Sarua, et al. IEEE Transactions Electron Devices, Vol. 53, Oct. 2006, pp. 2438 - 2447

ACRONYMS

HEMT: High Electron Mobility Transistor
2DEG: Two Dimensional Electron Gas