EM Simulation and Development of Wafer Level Micro-packaging Technique for GaAs-based RFMEMS Switches

Sandeep Chaturvedi[1], Member, IEEE, Sangam V. Bhalke[1], Mahadeva Bhat. K. [2], G. Sai Saravanan[1], R. Muralidharan[1], Member, IEEE, Shiban K. Koul[3], Senior Member, IEEE

[1]Gallium Arsenide Enabling Technology Center (GAETEC), Vignyana Kancha Post, Hyderabad-500069, India
[2]Solid State Physics Laboratory, Timarpur, Delhi-110054, India
[3]Center for Applied Research in Electronics, IIT Delhi, New Delhi-110016, India

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Abstract: We present here a technique for wafer level micro-packaging of GaAs based RFMEMS switches. The developed technique is simple yet effective as it has a very minimal effect on the switch performance. Effects of package cavity height and physical properties of the cap material have been analyzed by full wave simulation and the optimal parameters were used during fabrication.

INTRODUCTION

MEMS switches consist of delicate moving membranes which are also sensitive to moisture and external environment. It is therefore necessary to package these devices at wafer level itself to avoid damage to the membrane during singulation/assembly process. Various wafer bonding methods [1-4], including anodic bonding, thermo-compression bonding, adhesive bonding etc., have been proposed in literature for this kind of wafer level packaging. The anodic bonding method works very well for low resistivity substrates like silicon or glass but cannot be used in situations where the substrate has high resistivity like Gallium Arsenide. In thermo-compression bonding, one has to create specially designed signal vias for accessing the signal pads of the device, and these lead to increase in insertion loss which is the primary advantage of MEMS switches. The method proposed here falls in the category of adhesive bonding but is unique in the sense that it does not require signal vias and hence does not affect the insertion loss of the switch. Moreover, the proposed method is based on fabrication of individual cavities and then aligning and bonding them manually over the MEMS bridge area to protect the beam using an adhesive material. Thus, this does not require expensive wafer bonding equipment. Fig-1 shows the proposed concept. In this method the MEMS switches and the Microcaps are fabricated separately like any other packaging method. After fabrication, the Microcaps are singulated using a high speed dicing saw. Next, the individual caps are inverted and an adhesive material is applied at the interface area. Finally, the caps are carefully aligned covering the beam area, leaving the signal pad access and pressed together and cured. We have done full wave simulation of this packaging method using CST microwave studio EM simulator, and it is shown that the insertion loss degradation after packaging is less than 0.2 dB while the isolation of the switch is completely unaffected.

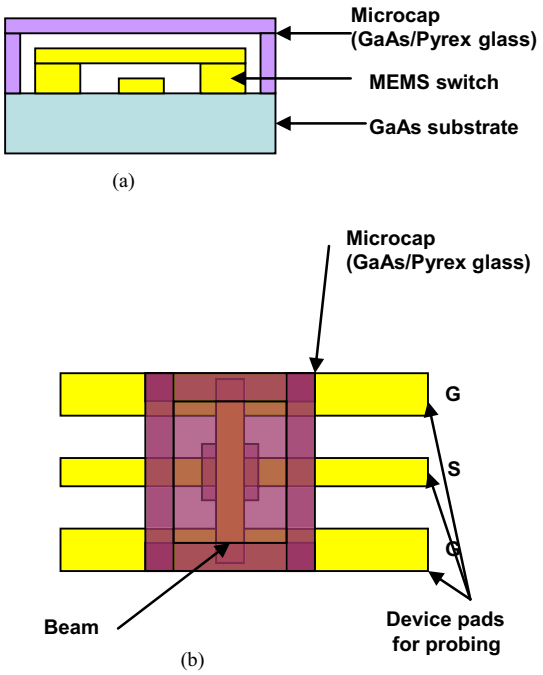


Fig-1: Proposed micro-packaging concept for GaAs based RFMEMS Shunt switch, (a) Cross section, and (b) Top view

SIMULATION

An RFMEMS switch structure with meandered beam, as shown in Fig-2, was taken for studying the effect of micro-packaging on its RF performance. This structure was fabricated at GaAs fab, GAETEC. We propose to incorporate the wafer level micro cap for this switch and similar structures for their protection during further assembly operations. The proposed cap structure is made in such a way that the sophisticated part of the switch, the beam, gets encapsulated while leaving the CPW pads accessible for on-wafer probing of the switch. The switch and the cap structure were simulated in CST Microwave studio Electromagnetic simulator. Two types of materials were considered for the proposed micro-caps, viz., 0.2mm GaAs and 0.7mm Pyrex glass. The depth of the cavity covering the beam area was varied from 2 to 50 microns to see the effect of vicinity of cap layer on the switch insertion loss and isolation.

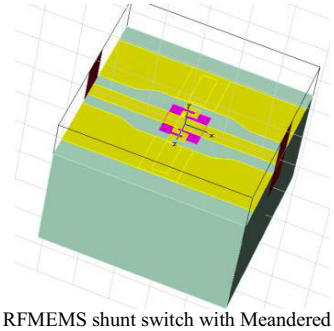
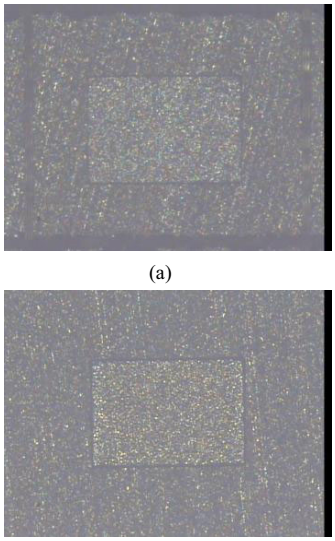


Fig-2: Capacitive RFMEMS shunt switch with Meandered beam

FABRICATION

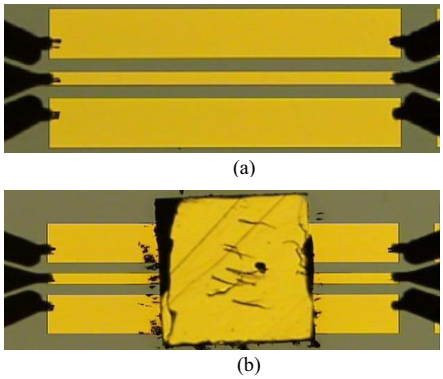
GaAs based micro-caps have been fabricated using plasma enhanced dry etching process. Different cavity depths in the range of 5-20 micron have been fabricated as shown in Fig-3. For initial verification, these caps were aligned and attached over a 50ohm CPW line using non-conducting epoxy as shown in Fig-4. The insertion loss of a through line was measured prior to and after placing the microcap.



(a)

(b)

Fig-3: Microcap cavities fabricated on 200um thick GaAs substrate with depths of 5um and 20 um



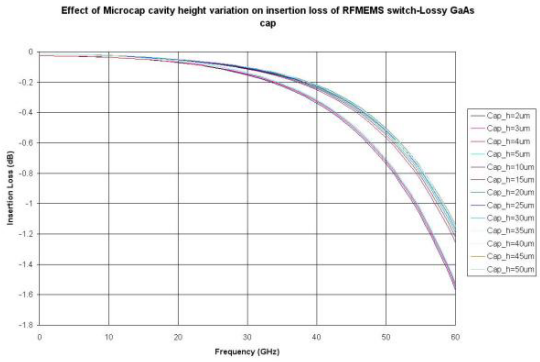
(a)

(b)

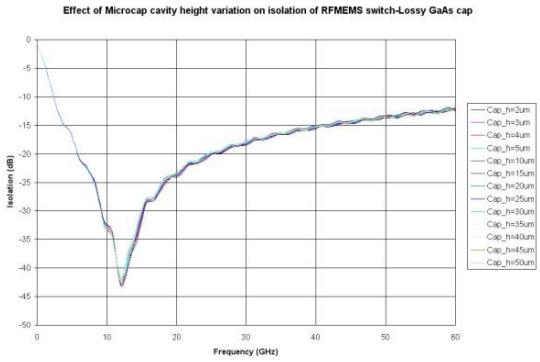
Fig-4: Reference CPW line (a) used for characterization of micro-cap (b) on insertion loss

RESULTS AND DISCUSSION

Fig-5 shows the simulated effect of micro-packaging with GaAs as the cap material. It can be seen that at a benchmark frequency of 40 GHz, the worst case simulated insertion loss is 0.32dB at a cavity depth of 2 microns. The isolation performance is unaltered.



(a)

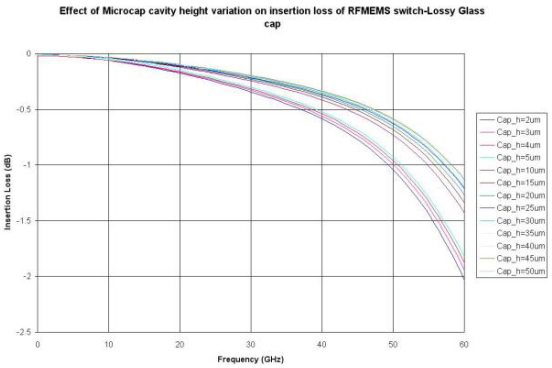


(b)

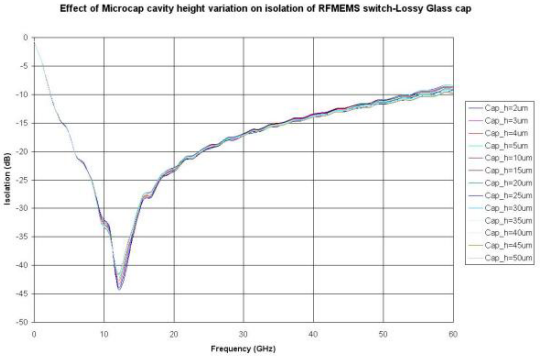
Fig-5: Effect of Micro-package cavity height on (a) insertion loss and (b) isolation performance of RFMEMS switch for lossy GaAs cap

Fig-6 shows the simulated effect of micro-packaging with Pyrex Glass as the cap material. The worst case simulated insertion loss is 0.58dB at cavity depth of 2 microns at 40 GHz. The isolation performance is unaltered once again. The slight increase in insertion loss is attributed to higher substrate losses in case of Glass.

Figure-7 shows the insertion loss of a CPW line (Fig-4) without cap and with GaAs microcaps with depths of 5 and 18 microns. It can be seen that (i) the microcap has a very small effect on the insertion loss and (ii) as the cavity height reduces the insertion loss increases, as predicted by simulation.



(a)



(b)

Fig-6: Simulated effect of Micro-package cavity height on insertion loss and isolation of RFMEMS switch for lossy Pyrex Glass cap

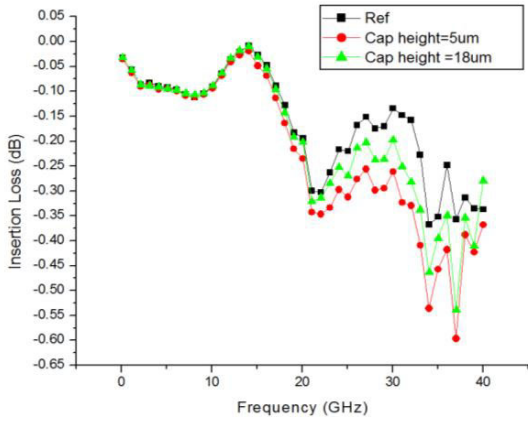


Fig-7: Effect of micro-cap on the insertion loss of a CPW line

ONCLUSION AND FURTHER SCOPE OF WORK

A simplified and effective method for wafer-level micro-packaging has been proposed. The simulation shows that this method can produce wafer-level packaged RFMEMS switches with least degradation in their performance. At present we have done the verification of effect of the propsed Micro-caps (made with GaAs) on insertion loss of a simple CPW line. It is further proposed to seal the actual working RFMEMS switches with these Microcaps and verify the effect on insertion and isolation of the switch. It is also proposed to repeat the same experiment with Pyrex glass based caps which are currently under fabrication.

ACKNOWLEDGEMENTS

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REFERENCES

[1] Chao C. H. and Pan C. T., "*Microcap Selective Packaging through Flip Chip Alignment*", NSTI-Nanotech 2004, pp. 472-475

[2] Seok S. et al., "*A novel packaging method using wafer-level BCB polymer bonding and glass wet-etching for RF applications*" Sensors and Actuators A 147,2008, pp. 677–682

[3] Iannacci J. et al., "*Electromagnetic optimization of an RF-MEMS wafer-level package*", Sensors and Actuators A 142, 2008, pp. 434–441

[4] Kim Y-K, et al., "*Low temperature epoxy bonding for wafer level MEMS packaging*", Sensors and Actuators A 143, 2008, pp. 323–328

ACRONYMS

RFMEMS: Radio Frequency Micro Electro Mechanical System

EM: Electro Magnetic

CPW: Co-Planar Waveguide