N-polar GaN-based highly scaled self-aligned MIS-HEMTs with state-of-the-art $f_T.L_G$ product of 16.8 GHz-µm for mixed signal applications

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Abstract

In this paper, we describe a gate-first self-aligned MBE InGaN regrowth methodology for fabricating N-polar GaN-based MIS-HEMTs which exhibit ultra-low contact resistances of 23 Ω-µm, which is comparable to the lower band-gap technologies. These devices, not only show state-of-the-art $f_T.L_G$ product values of 16.8 GHz-µm for 130 nm gate-length for GaN, but also show exceptional performance at low supply voltages (V_{DS} = 500 mV), thereby making GaN competitive not only to wide band-gap materials like SiC but also to low band-gap technologies by InGaAs HEMTs and InSb by having low knee voltages, high drive currents while still demonstrating relatively large breakdown voltages for unipolar (non-CMOS like) operation.

INTRODUCTION

AlGaN/GaN HEMTs have been successfully implemented as a high power high frequency technology due to their high density of states and velocity [1-2]. In the past however, most experiments were done on the Ga-face GaN with little attention given to N-face due to growth issues. After recent advances in MBE [3-5] and MOCVD [6] growth of N-polar GaN, it has been demonstrated that N-face devices have several potential advantages over Ga-face like the ability to achieve low contact resistance [7] and a natural back-barrier for electron confinement which can enhance the rf performance of GaN devices beyond the Ga-face capabilities. Some recent power data on N-polar GaN HEMTs has been shown to match with Ga-face [8], but little improvement has been demonstrated.

In this paper, we investigate a self-aligned design for N-polar MIS-HEMTs with MBE regrowth of graded InGaN-based contact layers to not only highlight the advantages of N-face, but also demonstrate current-gain cut-off frequency data out-performing the existing state-of-the-art Ga-face results for gate-lengths greater than 120 nm.

DEVICE DESIGN AND FABRICATION

The device structure consists of a standard N-face structure with $Al_{0.3}Ga_{0.7}N$ barrier, AlN interlayer and 10 nm GaN channel with 5 nm MOCVD grown SiN gate insulator with 2DEG sheet resistance of 600 Ω/sq (Fig. 1a). The band diagram with the regrowth is shown in Fig. 1b. The graded and n-doped AlGaN at the back helps keep the Fermi level away from the hole trap near the valence band of GaN [5]. The gate-first process was adapted from the InGaAs MOSFET technology reported by Rodwell et. al. in 2008 [9-10]. The process involves blanket deposition of $W/Cr/SiO_2/Cr$ followed by e-beam lithography of gate-fingers using a negative resist (MA-N 2403) and subsequent etching of *Cr* which acts as a mask for etching the rest of the gate stack. Multiple layers in the gate-stack are chosen to maintain etch-selectivity while etching each layer with the goal to form a refractory-metal gate capped with SiO_2, so that the metals are not exposed to the MBE chamber during regrowth. PECVD SiN_x sidewalls are formed around the gate by blanket deposition and vertical dry-etch. Graded InGaN layers (40 nm) with InN cap (10 nm) are regrown in the access regions by plasma-MBE to achieve R_C = 23 Ω-µm. The cross section SEM of the regrown area is shown in Fig. 2 and more details about the regrowth process are given in [7]. The subsequent transistor fabrication involves height selective etching of InGaN from the top of the gate to isolate source and drain [11] and deposition of Ti-based non-alloyed contacts with L_{SD} = 1µm.

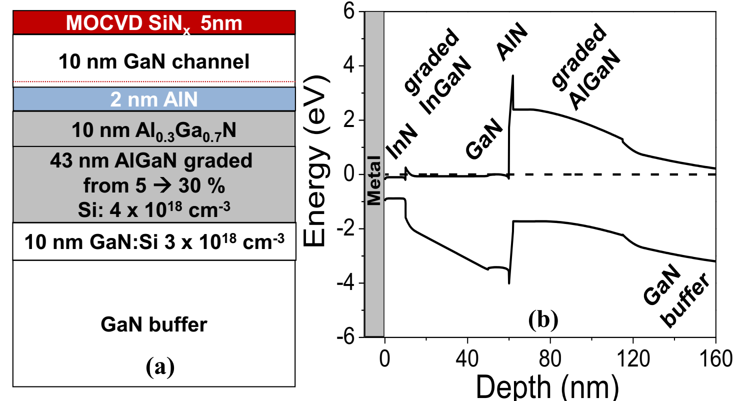


Figure 1. (a) Epitaxial layer structure of the device. (b) Band diagram of the device structure with regrown InGaN layers on top showing very little barrier in the path of electrons from the ohmic contact metal.

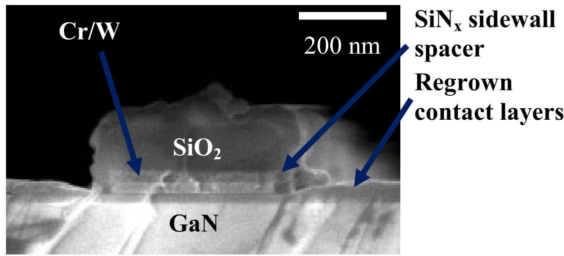
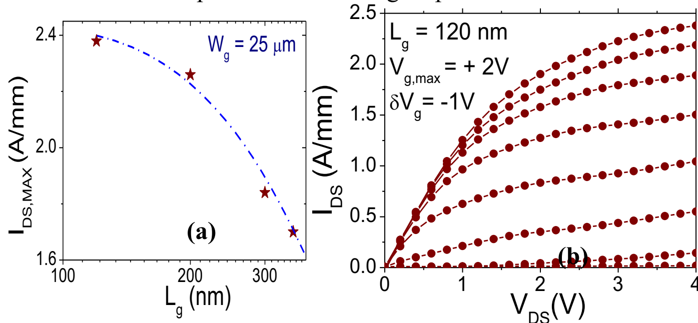


Figure 2. Cross section scanning electron micrograph of a gate stripe after the regrowth. The regrowth occurs all the way to the gate edge without significant shadowing.

MEASUREMENT AND ANALYSIS

DC measurements are performed on the fabricated devices and the current is observed to scale very well with gatelength as shown in Fig. 3a. Since the gatelengths are fairly large as compared to the mean free path of GaN, no ballistic efefcts have been observed. The device with L_G = 120 nm shows excellent DC-IV characteristics and transfer characteristics with I_{MAX} = 2.4A/mm and g_m = 530mS/mm at V_{DS} = 5V and $I_{D,sat}$ = 0.6A/mm and g_m = 350mS/mm at V_{DS} = 500mV (Fig. 3). These values are state-of-the-art not only compared to AlGaN/GaN systems but to several other low bandgap technologies. As shown in Fig. 4, the extrinsic g_m remains relatively flat with I_{DS} which indicates that the g_m-lowering due to a source choke has been effectively eliminated by a self-aligned structure. As expected from the self-aligned device structure, the device did not show any DC-RF dispersion for 200 ns gate pulse.



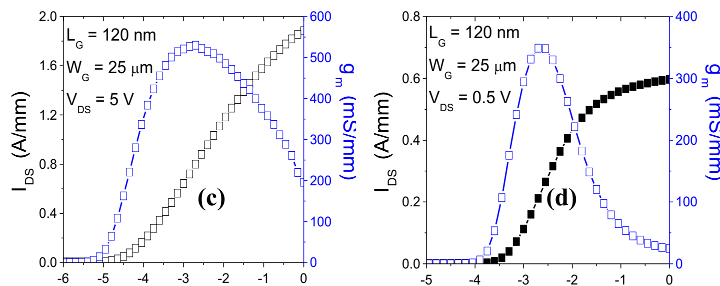


Figure 3 (a) Variation of maximum saturated drain current with gate length. (b) DC I-V characteristics for L_G = 120 nm showing I_{MAX} = 2.4 A/mm. Transfer characteristics of the device at (c) V_{DS} = 5 V and (d) V_{DS} = 500 mV.

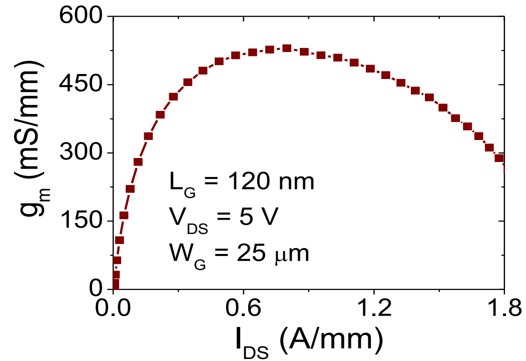


Figure 4. g_m as a function of drain current showing minimal transconductance-collapse due to source choke.

Small signal measurements were performed on Agilent 8361A Parameter Network Analyser and f_T and f_{max} of 132 GHz and 17.5 GHz were obtained for L_G = 120 nm (Fig. 5a). Small signal equivalent circuit was extracted to understand the cause for low power gain. Hence, the gate resistance, R_G and gate-to-drain capacitance, C_{gd} were extracted to be 1400Ω and 0.1pF/mm respectively. The relatively large value of R_G, attributed to a thin gate stack (100 nm) of W/Cr, was assumed to be the main cause of low f_{max}. Simulating the same equivalent circuit with R_G = 5Ω yielded an f_{max} value of 250 GHz, thereby confirming the hypothesis.

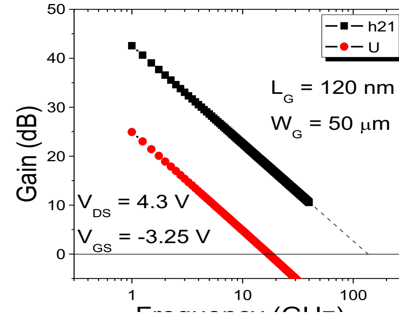


Figure 5. Current gain and unilateral power gain vs. frequency showing f_T of 132 GHz and and f_{max} of 17.5 GHz for L_G = 120 nm

Self-aligned T-gate process was then developed to reduce the gate resistance. The fabrication process involves height-selective etching of e-beam resist after the access region regrowth to create a resist spacer around the *W/Cr* footgate, wet-etching of SiO_2 from the top and e-beam lithography of the top T-gate. T-gate process has been tested on devices with L_G = 1μm resulting in f_T and f_{max} of 10 and 21 GHz respectively at V_{DS} = 4V, which is similar to the f_{max} values for non-self-aligned devices for similar drain bias (Fig. 6). Measurements were not done at higher drain biases to prevent breakdown. Fabrication of sub-micron devices with the top-gate process is ongoing and f_T and f_{MAX} of 40 GHz and 70 GHz respectively have already been obtained. Further scaling by optimizing the SiO_2 wet-etch is being done and will be presented at the conference.

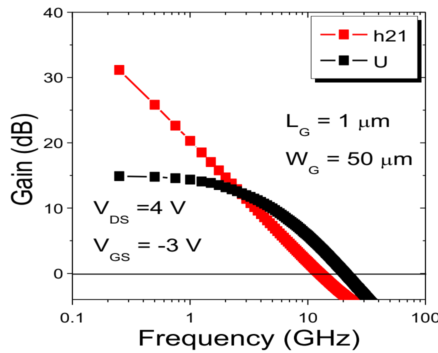


Figure 6. Current gain and unilateral power gain vs. frequency showing f_T of 10 GHz and and f_{max} of 21 GHz for L_G = 1 μm with self-aligned T-gate process on sample with GaN channel thickness = 25 nm

To assess the quality of the scaling process with the self-aligned technology, variation of f_T was studied with respect to gate-length. As seen in Fig. 7, f_T scales as $1/L_G$ demonstrating the advantage of a self aligned structure in minimizing the effect of parasitic elements. It was also observed that f_T was relatively flat with drain bias indicating elimination of drain delay in a self-aligned structure.

CONCLUSION AND BENCHMARKING

Self-aligned fabrication of N-polar GaN/AlGaN HEMTs has been demonstrated. Excellent DC-characteristics were measured with state-of-the-art $I_{DS,sat}$ of 2.4 A/mm and very flat g_m profile with drain current indicating successful elimination of parasitic components. The rf-metrics also scale well with gate length up to 120 nm indicating effective scaling of parasitics.

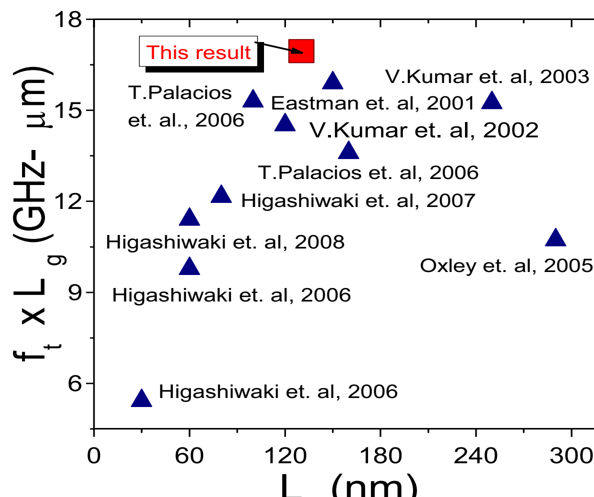


Figure 8. Comparison of our best self aligned device with the state-of-the-art results for GaN technology highlighting effective delay reduction by self-aligned device structure.

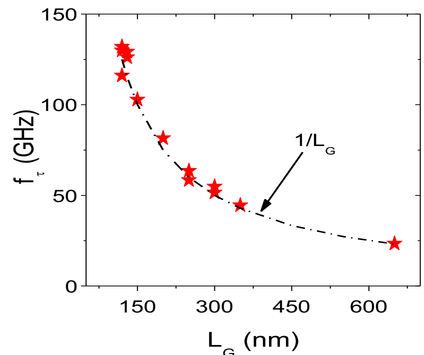


Figure 7. Current gain cutoff frequency vs. gatelength showing $1/L_G$ behavior indicating scaling of delays along with gate length scaling for a self-aligned device.

The above results have been compared with the state-of-the-art rf results published by groups working on Ga-face HEMTs. Fig. 8 shows that we have been able to achieve record $f_T.L_G$ product of 16.8 GHz-μm for submicron HEMT technologies on GaN. As can be seen in Fig. 9, total delay ($1/2\pi f_T$), which is close to the intrinsic gate delay for self-aligned devices, scales linearly with L_G and is comparable to GaAs/AlGaAs and InGaAs/AlGaAs systems and within 0.4ps of the intrinsic gate delays reported by lower bandgap technologies like InGaAs/InAlAs and InAs/AlSb systems. With further scaling with the T-gate process, excellent rf performance can be achieved.

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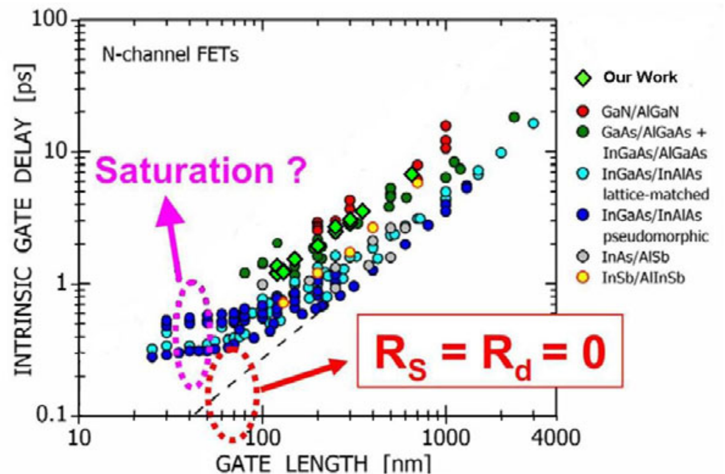

Figure 9. Comparison of total delay ($1/2\pi f_T$) in N-polar GaN-based self aligned transistors with other technologies. Figure taken from R. Chau et. al., Technical Digest, CSISC 2005, pp. 17-20 (Si MOSFET points have been removed for clarity).

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ACRONYMS

HEMT: High Electron Mobility Transistor
MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor
N-face(polar): Nitrogen-face(polar)
MBE: Molecular Beam Epitaxy
MOCVD: Metal-Organic Chemical Vapor Deposition