Selected technological improvements of SiC power devices in order to achieve high performance combined with outstanding ruggedness

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Abstract

The following paper will address several aspects of SiC power device technologies which are mainly related to challenges arising from peripheral topics like packaging, e.g.; or are triggered by reliability issues. It will be sketched how devices can be optimized by design and improved processing in order to enhance the reliability. A critical discussion will be dedicated to power density considerations while developing SiC power devices. Finally, limits and alternatives of resp. for today's packages regarding the switching speed will be shown and discussed.

INTRODUCTION

Silicon carbide based power semiconductors are still believed to be key components for future highly efficient energy conversion systems in many existing and emerging markets [1, 2, 3]. Anyway, the broad commercial success is still open, blocking points are besides the high component costs also difficulties with simple plug and play approaches as favored by many users. The contribution will sketch which not directly to the device related topics must be taken into account while manufacturing successful SiC components.

The expectations regarding the use of SiC components are high, the most prominent features of SiC should be

- high temperature performance
- very fast switching
- lower losses than silicon or higher power densities

However, in order to fulfill these challenges not only the pure chip development is of importance, but also other parts like packaging technologies with its cycling limitations at elevated temperatures [4] or new degradation phenomena e.g. caused by overgrown micropipes have to be considered [5]. Other packaging technologies in turn have effects on the chip technology and thus, a closed loop approach for taking into account those additional topics seems to be important as well. Limits are today the removable power density defined by the thermal resistance of a given package and for high speed operation the parasitic inductances arising from bond wires.

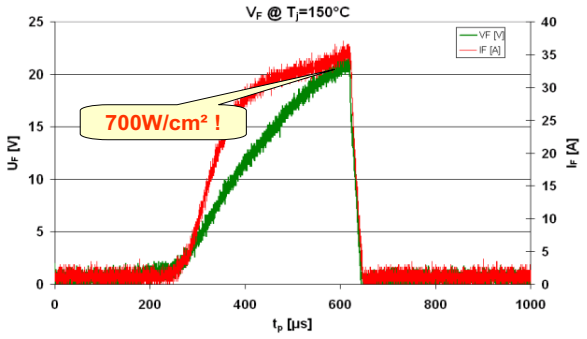
While for the application it seems to be of advantage to utilize higher temperatures this trend is critical regarding the reliability. For those aspects both, the temperature swing and the absolute steady state temperature in the application are dangerous. Mainly in surge mode or during other short time events (e.g. short circuit or avalanche) in the application the junction temperature in SiC components can increase to a couple of hundreds of °C. From functionality point of view – and this is the benefit of SiC – the device can withstand it. However, the overall integrity of the assembly will suffer and thus, the current efforts are directed to a reduction of peak temperatures in the device. It will be shown in the following paragraphs how this can done by design and technology in parallel.

In order to keep the devices costs small and footprints of chips lower that classical silicon SiC devices should operate at much higher current densities. However, again limitations coming from the available cooling opportunities which have to remove the higher power densities and from the capabilities of bond wires for feeding in the high currents at a relatively small area have to be considered. Finally, the fact that smaller chips have a non-linearly higher R_{th} than larger die represent a next hurdle for the full use of SiC inherent advantages and will be discussed shortly after device type specific issues.

RELIABILITY AND HIGH POWER DENSITIES IN SIC SBD'S

As already mentioned in the previous paragraph it is mandatory to limit peak power densities and thus, the maximum temperatures in a component in order to achieve a high reliability. This is a severe challenge mainly for the state of the art SiC devices due to the inherent high power densities already under nominal operation conditions combined with the ohmic resistance like increase of the losses with temperature which is an device physics related feature of unipolar components like SBD's, MOSFETs or VJFETs. For addressing this challenge design improvements can be very beneficial. Examples for diodes are modern diodes with an in-built surge current handling capability by

bipolar boosts (see Fig. 1). As can be seen from the graphs the peak power density can be reduced by a factor of two from 700W/cm² down to 350W/cm² which make such diodes not only more comparable to the silicon performance in such modes, but also provide an improved reliability since absolute temperature cycle ΔT in operation can be dramatically reduced which will increase the lifetime [4].



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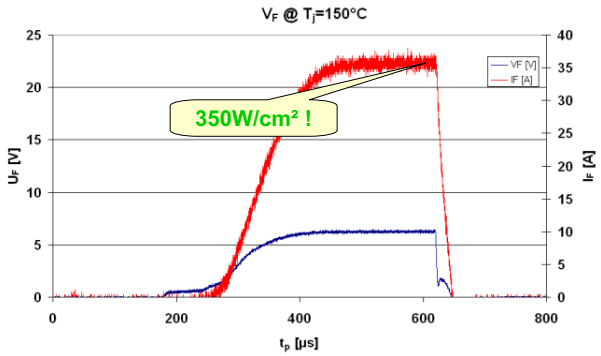

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Fig. 1: Comparison of the peak power density under surge mode for diodes without bipolar boost (a), left) and diodes with bipolar boost (b), right), a higher power density can be directly transferred into a higher peak temperature

Comparable considerations like for elevated temperatures exist for the wish to achieve high power densities in SiC components. It is favorable to have high current densities since then a chip can be small and therefore cheap, anyway, the resulting power density increases with the square of the current density. On the one hand it is known that SiC has a very good thermal conductivity and thus, the resulting power losses should be easily removed, however, thermal simulations revealed a strong contribution of the backside solder process to the overall thermal impedance, acting simply spoken like a wall for the heat flow. New disruptive assembly flows are mandatory to handle this. In the third generation of Infineon diodes this topic is addressed by avoiding solder layers at all [7]. This technology does not only offer a reduction of the R_{th} by a factor of 2, but in addition a further limitation of the internal peak temperatures as shown in Figure 2 what is again beneficial for the long term stability of the device in its package.

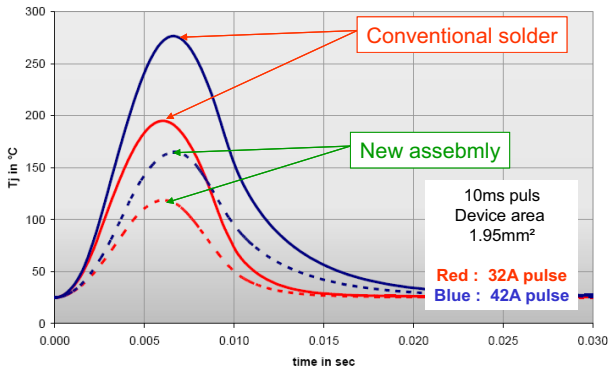


Fig. 2: Peak temperatures in the devices during pulse current stress, comparison of standard solder assembly and a new solderless solution

This new packaging technology allows current densities up to 700A/cm² in discrete packaging solutions. Such high current densities under normal conditions will also result in very high power densities. Cooling becomes very important and mainly the removable power densities of available cooling methods (between 250W/cm² for air cooling and up to 600W/cm² for water cooled systems) have to be considered in the case of assembly techniques for higher power ratings like modules e.g. In those setups lower current densities apply and again there is the situation that it is not possible to utilize the full power handling capability a SiC chip itself is able to provide due to limits of the periphery.

HIGH TEMPERATURE OPTIMIZATION OF SIC VJFETS

High temperature semiconductors are required by several applications like deep hole drilling, aircraft industry or even automotive solutions. The motivations are different, deep hole drilling e.g. is characterized by very high ambient temperatures and thus, the case temperature is already higher which forces the use to increase the junction temperature of device in order to remove the heat created by losses in the semiconductor. Other applications would like to take advantage of a higher difference between case and junction temperature what allows for a given R_{th} a higher amount of removable heat and thus, more power for a given frame size. Today mostly the packaging reliability limits the maximum temperature, however, mainly for high blocking voltages also the semiconductor physics of silicon become noticeable by strongly increasing leakage currents which exceed acceptable limits above 200..250°C, depending on the actual blocking voltage. SiC can theoretically operate even above 1000°C, however, it is worth to discuss a reasonable target for a high temperature chip while again taking into account some boundary conditions coming from the environment of the chip.

Assuming the applications where the higher ΔT between case and ambient should be used it is important to include in the considerations the resistive behavior of the mostly unipolar SiC based switching components. Resistive behavior means an increase of the R_{on} with temperature, mostly governed by an exponential dependence according to the formula

$$R_{on} \propto T^{\alpha} \qquad (1)$$

with the exponent ranging from 1.5..2.5, depending on the actual device structure as discussed below. Taking this into account it becomes obvious that an unlimited increase of the maximum temperature will end up with a thermal runaway since the losses will increase to values exceeding the possibilities of the package. For typical values of the used R_{th}, the R_{on}=f(T) function and typical case temperatures in such applications it can be derived that the optimum maximum temperature is nearly always between 200°C and 300°C as schematically shown in Figure 3 and thus, a mid term development target should also be directed into this interval. Higher maximum T_j would bring no further benefit because the current handling capability will decrease again.

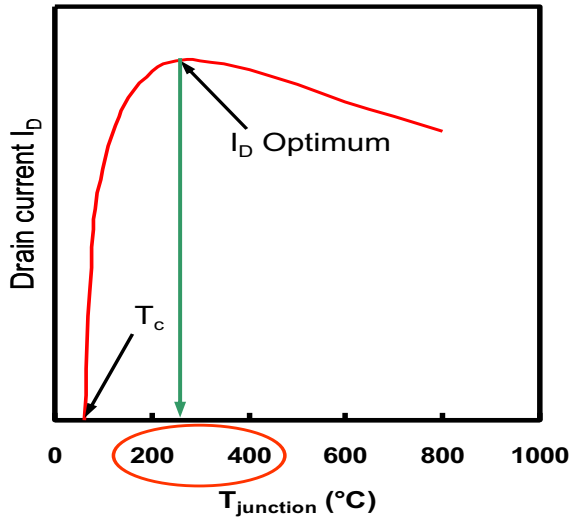


Fig. 3: Schematic estimation of an optimum T_{jmax} for achieving a maximum current for a unipolar semiconductor component, parameters are T_{case}, R_{on} =f(T) and R_{th}

Another way to improve the behavior of unipolar devices with temperature in to tune the exponent for the increase of the on-resistance with temperature as expressed in eq. 1. The lower the exponent the lower the increase of the R_{on} and thus, the increase of losses which follow the function

$$P_{tot} = I^2 \times R_{on}(T) \qquad (2)$$

For doing this the lateral-vertical concept we are following in our VJFET developments offers certain degrees of freedom in the design. Since the control region can be designed fully independent of the drift region we can use high doping levels in this region which have a considerably smaller increase of the resistivity with temperature due to changed scattering mechanisms and incomplete ionization. As shown in Figure 4 the achieved exponent is much lower than for competing structures or the established silicon MOSFET technology at higher blocking voltages.

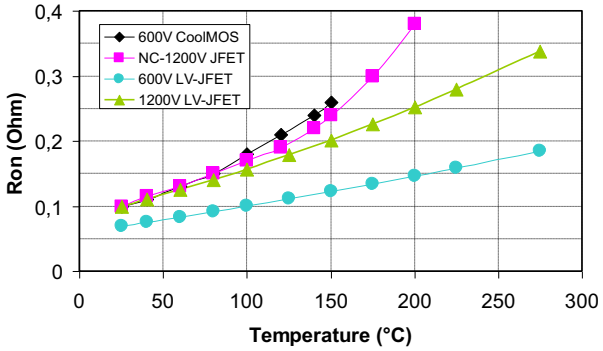


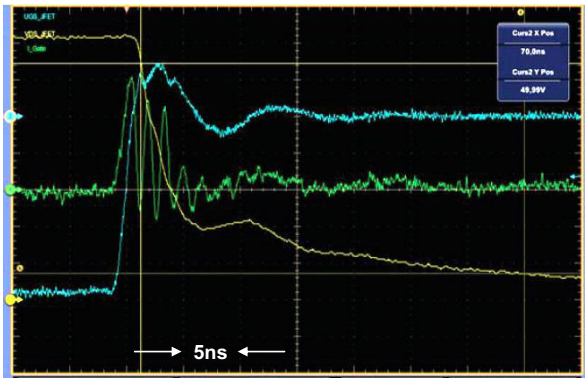
Fig. 4 :Increase of the on-resistance with temperature for different device type like a silicon CoolMOS™, a normally off SiC VJFET and two types of SiCED's lateral-vertical channel VJFETs

Also compared to other unipolar SiC transistor technologies a certain benefit is obvious. It should be noted at this point that for the losses in the application the R_{on} at operating temperature (e.g. 175°C) should be considered and not the often very attractive value at room temperature. By doing this comparisons do look like different, also with respect to silicon IGBT's e.g. which have a nearly temperature independent forward voltage drop and thus, at operating temperature the performance advantage of SiC FET's regarding static losses is much lower.

SiC MOSFET are often promoted with a small increase of R_{on} as well, however, for those components this behavior originates from the poor interface quality. Once this topic is addressed and solved SiC MOSFETs will behave pretty much comparable to the described JFET devices.

Another goal of silicon carbide based power electronic systems is to increase switching frequencies in order to reduce the size of passive components. However, higher switching frequencies are often combined with steeper switching transients (dv/dt and di/dt) and thus, EMI issues become more and more important. One source of the disturbing oscillations are parasitic elements of the used package and especially bond wires represent a considerable contribution to inductances; mainly if the switching frequencies become higher than several hundreds of kHz. For the switching of high currents in the ns time scale the source inductance is crucial since due to the induced bias the applied gate voltage is compensated and therefore, unwanted

turn-on and –off and an overall prolonged switching period can be observed like illustrated in Figure 5 a) in case of a VJFET with a standard TO220 package.



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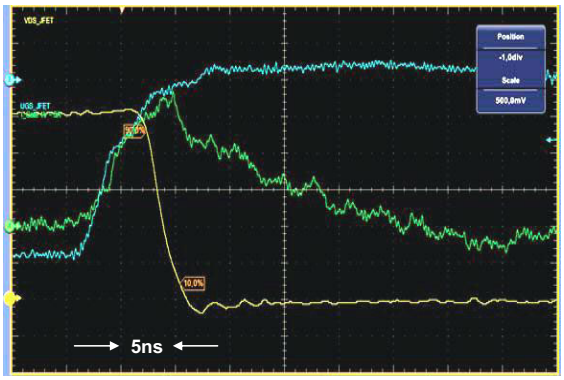

b)

Fig. 5: Influence of wire bonds on oscillations of terminal signals and switching speed for SiC VJFETs in the ns range (scale 1ns/div), same chip type, upper figure (a) standard wire bond in TO220 and lower figure (b) wire free assembly, green curve =gate current I_G (500mA/div), yellow curve (20V/div) = Drain-Source voltage V_{DS} and blue curve (5V/div) = Gate-Source voltage V_{GS}

Figure 5b shows the same chip in a new assembly without wire bonds. Clearly a much smoother V_{GS} behavior can be seen and thus, also the drop of the drain bias can be realized much faster. As a consequence it can be stated that also with respect to the utilization of higher switching frequencies a parallel developed of the peripheral building block like the package is mandatory for success.

Finally a critical consideration regarding the benefits of very low R_{on}x A values will be made. For the user, the current handling capability is important and mainly for small die and very low R_{on}x A the additionally gained current handling capability is surprisingly low even if the R_{on}x A is for example reduced by a factor of 2. This is again related to limits coming from the removable power density (please note the statements in the diode section) and for small chips to the non-linear increase of the thermal resistance. For the practical use it is therefore important to make a reasonable balance between the efforts to achieve a goal in terms of numbers and the practical use of it.

CONCLUSIONS

In the previous paragraphs selected topics are highlighted which are in the authors opinion important for a full picture about the use and the benefits we can gain from new technologies like SiC power devices. Important to note is that the development of a new chip technology should be in parallel with improvements of peripheral technologies like packaging e.g. in order to make sure a full use of the benefits provided. Examples were given for modifications of the contact technology in order to avoid parasitic inductances. Also reliability considerations should be integrated in the development from the early beginning, for this topic both, the device design and the packaging technology can help to address upcoming challenges arising from very high power densities and/or higher peak temperatures compared to the well developed silicon technology.

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ACRONYMS

MOSFET : Metal Oxide Semiconductor Field Effect Transistor
P_{tot} : total device losses
R_{on}: on-resistance
R_{th} : thermal resistance
SBD : Schottky Barrier Diode
SiC: Silicon Carbide
VJFET: Vertical Junction Field Effect Transistor