Modular Solid State Technologies for a Multi-functional System Integration
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Abstract
A trend in system integration aims for human centered and environmental solutions and therefore need to focus more on multifunctional interfaces for smart systems in order to develop tailored solutions. A modular merge of different technology concepts CMOS, MEMS, HF ICs (III-V, II-VI…) 3D system integration on interposer, wafer and board level takes place in order to design application oriented interfaces amongst the major existing technologies for such a multi-functional systems integration. First add-on technologies will be the dominant system integration technology in the near future and in a second wave a kind of modular solid state technology might develop building the base for high-performance multi-functional systems.

INTRODUCTION

The trend towards miniaturized multi-functional devices is clearly visible and conceptual ways to follow are well described in literature (ENIAC, www.eniac.eu and European technology platform for Smart System Integration EPOSS, www.smart-systems-integration.org). Specialized solution for systems combining conventional logic and memory devices and interacting with them in a systems oriented manner will enable new visionary products and are of paramount importance for the technology roadmaps described in literature. Examples are complex moving object recognition or integrated personalized medical diagnostic systems.

After decades of system integration technologies focusing on device technologies and their networks – from televisions to computers and cell phones – future micro system integration is probably to center more on humans and the environment. With its trend of increasing system integration level, on wafer level Moore’s Law will become less important in the future for such a task. So-called “More Moore” and in particular add-on technologies will play major roles in multi-functional systems integration in the coming years.

Add-on technologies are a possibility to further approach the area of “More than Moore” by monolithic integration of sensors (movement, mass, imaging…), detectors (photodiodes…), high-quality passives (high-Q inductors…). They aim monolithic integration of electrical and non-electrical functions with conventional silicon (mostly CMOS) technology in order to reach new functionality on system level based standard wafer products. They are already well known since years and developed further by a number of research institutions and companies mostly developing the technologies still for special purpose product solutions [1-6]. Therefore add-on concepts have already solved many problems in the last years, but mostly in a very specific manner tuned to each application problem, without using such possibilities of a modular or generic More-Than-Moore strategy.

Present work with add-on technologies is being carried out in mostly two main directions. In the first approach, functional layers are placed on previously made wafers and then structured during system integration. These layers can contain other materials or non-CMOS-compatible materials, making integration of additional functions (for example, wave guides, photonic devices or sensor effects [1-3]) possible. The second approach is vertical system integration (3D integration) on the wafer level [4]. This makes it possible to have a combination of chips from various functional groups, which cannot be economically integrated in a monolithic way because of the material used or related costs involved. High-frequency ICs can be combined with silicon or MEMS chips in an interposer or wafer level integration. Additional functional layers can be integrated to support such on-top or add-on system integration processes.

MOTT (Multifunctional On-Top Technologies) aims to develop a modular add-on technology system approach for enhancing the functionality of standard silicon chips, MEMS and CMOS technologies. Merging technologies in the frame of such MOTT approaches is perhaps only the beginning of a multi-disciplinary fusion process. MOTT technologies will have to be further developed in a multifunctional modular approach and somehow merge with “Beyond CMOS” approaches in order to apply it in a broader product range. This might lead to a main stream modular solid state technology for system integration in near future.

MULTIFUNCTIONAL ON-TOP TECHNOLOGIES MOTT
Multi-functional on-top technology integration can profit much if conceptually structured in device, functional and integration level in order to allow a system oriented design and manufacturing of multi-functional optimized systems as
summarized in table 1 and explained in more detail in the following.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Definition of MOTT Technologies</th>
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<tr>
<td>Level Tec</td>
<td>Technologies</td>
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<tr>
<td>Device / Front-end / pre-processing</td>
<td>fabrication of active devices (single-crystalline poly-crystalline, amorphous, polymer) sensors and actuators, via-first, etc.</td>
</tr>
<tr>
<td>Functional / Mid - Processing</td>
<td>passives, special system elements (piezo, fluidic, optic, magnetic, bio etc.) “functional-via”, organic electronics, polytronics, etc.</td>
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<tr>
<td>Integration / post processing</td>
<td>post-processing (front- and backside processing, membranes, cavities, “add-on-MEMS functionality”), SLIT Technology, 3-D VSI, post-processed vias, thinning and handling of wafers, dicing, organic electronics polytronics etc.</td>
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MOTT (Multipurpose On-Top Technologies) is to develop such modular system approaches for enhancing the functionality of standard silicon chips, MEMS and CMOS technologies. Back to internal research at Fraunhofer the multi-functional on-to technology approach has been formulated in a technological concept study MOTT in 2008. It bases on the combination of the more monolithically oriented More-than-Moore view of ENIAC in particular the part of the Add-on technologies with the more systems-oriented view of EPOSS both approaches can be merged towards such multi-functional On-Top Technology) ready to base on a standard CMOS and even on a standard MEMS wafer in order to increase functionality starting at the front-end up to adding functionality by post-processing in the back-end or back end of line in a modular manner.

In order to establish the compatibility with standard Silicon and MEMS technologies the following properties of on-top technologies are requested.

1) Pre-processing is related to the device level in the MOTT concept. Processes compatible with Silicon CMOS processing are required to be applicable on wafer diameters of 200mm and above. Therefore only a limited spectrum of allowed materials can be used for processing in the device level.

2) Mid-processing (MOTT functional level). Additionally to pre-processing low temperature processes need to be developed, to enable their systems-oriented post-application on partial or fully processed CMOS and MEMS wafers. Functional layers are deposited on the wafers in a layer-by-layer integration for additional functions. This can be achieved in a pre-BEOL level, but these functions will have to be routed and interconnected in a 3D approach in the BEOL afterwards. A more complex alignment of BEOL masks need to be considered.

3) Post-processing (MOTT Integration level).

In order to complement the pre- and mid-processing the routing, re-distribution in the Interconnect and pad levels is the core problem of 3D integrated modular systems. It may be compared to the human brain, where the device and functional level is represented by the neuron and the electro-chemical interface section of the neurons to the nerve interconnect-lines. However the performance of the brain system is mainly reached by the nerves as interconnects between the neurons and the ability of neurons to handle the numerous nerve interconnections to different neurons at the same time. Back to the 3D technology significant impact can be expected in this integration level from substrate-handling and —preparation as well as all the 3D on-wafer processing technologies like SLIT and TSV for vertical system integration (VSI) []. All of these interconnect processes are performed in a BEOL level on already completely manufactured integrated circuits, but they connect now to the lower MOTT device and functional levels to result in an optimized overall system significantly overcoming the 3D integration and packaging approaches of un-prepared devices in the conventional non-modular approaches.

These three processing regimes distinguish significantly in their frame conditions in processing.

In the device level three different processing types can be distinguished. For the single crystalline case we need to consider only materials not disturbing the silicon processing quality (i.e. no copper, causing recombination centers of free charge carriers etc.). The thermal budget is still possible to reach up to approximately 750°C. In this level functional material layers and device processes with critical dimensions reaching the nano meter dimensions can be connected with standard technologies. Materials can be deposited directly on the mother substrate allowing single-crystalline add-on structures for special purpose sensing, HF, and NEMS to be generated. The deposition could preferably be done by self-organizing processes such like selective epitaxy, atomic layer deposition (ALD). Beneath single-crystalline silicon different other layers (single-crystalline poly-crystalline, amorphous, polymer) may be deposited or coated (polymers) for devices [5,6].

In the functional layer the interconnections will be generated. Electrical isolation will be performed by amorphous materials and polymers. In this level the thermal budget is limited to approximately 400°C because of
Existing metal structures. Reaching the silicon surface of the base wafer is limited in this level. For this level therefore the add-on technologies need to be developed allowing the integration of 3-dimensional metallization stacks amorphous or polycrystalline, active and passive components (sensors, MEMS, NEMS, coils, capacitances, resistors etc.). Additionally in this level polytronic (organic electronic and biological technologies can be interfaced. The deposition methods in the device and functional level distinguish mainly in their thermal budgets.

For the integration level similar restrictions as in the functional level can be identified. Here processed wafers will receive additional components by the very flexible vertical scale integration (VSI) based on through substrate vias. Using SOI wafer it allows the access of the active single-crystalline area by the application of back-side etching methods in the frame of a post-processing.

The MOTT concept can be based on any substrate diameter and does not need necessarily to increase the wafer diameter to reach an economic product application.

As explained above a basic requisite of the realization of the MOTT concept is the establishment of a technology concept for the preparation and modification in the front-end level, open for interdisciplinary technology synergy in the front-end level and open for combinations with systems integration levels in the so-called back-end-of-line BEOL. In a second phase this might further develop towards a modular multi-functional front-end technology in future. Advanced MOTT technologies could provide solutions for Beyond CMOS, since they enable an early application of nano device technologies on standard wafer scale into products.

MODULAR SOLID STATE TECHNOLOGY

Integration of thin film processes, alternative semiconductor materials (SiGe, SiC, III/V, II/VI) or nanoscale structures by add-on technologies in the device level can be a route to a new multifunctional modular solid state technology in the future.

In the beginning of the integrated microelectronics era, materials science and electrical engineering teamed up with chemistry to create the microelectronics engineering. Over decades we developed this at that time “hetero- integration” to a very high expertise and towards a well-defined integrated silicon technology process. However, at the cost of further multi-disciplinary approaches such strict limitations have been route to success in silicon process technology and crystallized the field into only a few main process concepts for processors, controllers and memory over these decades. Only in the very last few years we have opened these strict rules when facing the stones of the red brick wall again and again. Now we allow different new materials in silicon technologies partially also enabling new functions. The synonym hetero-system integration is relative and valid only in the beginning. After some time of expertise and optimization such approaches will always lead to a kind of homogeneous process technology if additionally the cost models behind can be tailored to fit the product perspectives of the market in future. But this situation is similar to the silicon technology situation written down in the Moor’s law. Scaling has been predicted to continue as long as companies will make more and more money with it. The second aspect of balancing profitability and investment in semiconductor technologies is important for the further development of this possible multifunctional system technology.

A modular solid state technologies approach for future electronic systems could allow an additional degree of freedom in a soft transition or mutation of silicon technologies even into possible nano device technologies, organic electronics [5,6] or quantum electronics as addressed in the Beyond CMOS approaches.

Technologically the scaling of device technologies towards deep-submicron already led us into intensive studies of phenomenon in atomic and molecular dimensions in the frame of the different semiconductor technologies. Basic new innovative system integration concepts in the area of bio engineering, environmental engineering, human-machine interface request system solutions not solvable with systems engineering on the packaging level like boards or system in a package (SIP). The requirements for such multi-functional solutions together with performance requests like energy-autarkic, low power, low noise, high-band-width, high frequency and if possible all of them combined point to only one possible integration level being solid state technology systems. Only in the regime of highest integration all the system performance requirements can be fulfilled, unfortunately not using only one solid-state semiconductor technology. The basic semiconductor technologies need to be combined in an integrated modular technology platform.

Modern system technology requires multi-functionality and cost-efficiency and in many cases energy autarkic systems or very cost-efficient solutions, therefore even integrated in plastic or foil substrates. Selective structuring processes are developed to fulfill the requirement for high resolution i.e. integrated organic electronics in a foil as well as lithography of metal layers to fulfill the requirements of high performance power or data busses in the foil substrates. In the meanwhile it is possible to hetero-integrate full systems in a foil with organic integrated circuits and PV, display, passive components, flexible battery, thin silicon IC, as well as printed sensors and actuators [5,6]. The combination of several of these components will be the key to product application in near future.
The main focus is no longer only miniaturization but also modular solid state technology development with the aim of heterogeneous integration and the development of smart low power, energy autarkic multi-functional systems. With components manufactured by optimized modular process technology heterogeneous integration of functions from different technology environments will become possible and a significant advancement in functionality, flexibility and profitability will be reached.

CONCLUSION

Multifunctional and modular system integration technologies will in-particular be attractive to SME because of it’s flexibility and possibility to integrate high-performance add-on functions to available standard CMOS and MEMS products, but also for major semiconductor companies the modular approach and the chance to extend a silicon or MEMS processing technology towards a modular multi-functional solid-state systems integration technology will be a path to fast product development. The MOTT concept opens a possibility for small and medium series fabrication of high-performance systems

New approaches in particular such as MOTT and MSST aim for a modular integration of advanced functionality and new components into existing standard silicon and MEMS technologies merging with polymer functionalities and even plastic foil substrates. Together with 3D system integration this emerges to a key technology of high strategic relevance, rendering microsystems technology smaller, more powerful and more energy-and cost-efficient.

MSST concentrates back on the strength of microelectronics engineering in the early times being the merge of interdisciplinary topics (hetero-integration) into a technology process. It addresses the new challenges of a human and environment centered technology for cost-efficient and highest performance systems integration. We need now to add organics and biology to the materials science, electronics engineering and chemistry to overcome the existing borders to the human and the environment centered micro systems integration. A new MSST needs to merge many different functions from electronics over optics, towards, chemical and biological, fluidic and pneumatic functions. Systems of the future have to be lowest power and energy autarkic and recyclable as well as sustainable. The pressing loads onto the society to solve environmental, medical, social, nutrition related, security and logistical challenges can only be answered by a more general sustainable concept of multi-functional modular solid state technology development.

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REFERENCES


ACRONYMS

MOTT: Multifunctional On-Top Technology
MSST: Modular Solid State Technology