Investigation and Reduction of Leakage Current Associated with Gate Encapsulation by SiNₓ in AlGaN/GaN HFETs

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Keywords: AlGaN/GaN HFET, HEMT, dielectric passivation, leakage current

Abstract
The leakage current in AlGaN/GaN HFETs associated with gate encapsulation have been found to be sensitive to processing sequence and transistor layout. The main effect of the encapsulation by SiNₓ is an increase in the off-state gate leakage currents, which reach values in $1 \times 10^{-3}$ A/mm range or higher. Based on the comparison of transistors having different layout the effect is attributed to a residual stress in the encapsulating dielectric layer. The resulting differences in the gate leakage for different types of transistors were measured up to four orders of magnitude. The lowest values were obtained for transistor type, which has openings in both layers of SiNₓ formed in one etching step. The best average on-wafer value obtained in experiment is $3.0 \times 10^{-8}$ A/mm with standard deviation of $8.1 \times 10^{-9}$ A/mm. The optimized transistor layout and processing sequence has been used in our standard process for discrete GaN power transistors and MMICs. The results demonstrate stability and reproducibility of the developed approach.

INTRODUCTION

The use of dielectric surface passivation in AlGaN/GaN technology is caused by improvement in dc/rf dispersion characteristics of GaN-based HFETs [1]. This passivation layer induces mechanical strain, which depends on type of dielectric, thickness of the layer, substrate and conditions of deposition [2, 3]. The most common choice of dielectric in GaN technology for microwave and high power applications is silicon nitride. The SiNₓ is used for the two step lithography gate (“embedded” gate) realization. The MMIC fabrication process flow and the utilization of field plates in discrete microwave power transistors require encapsulation of the gate with the second dielectric layer. Beside these special requirements an encapsulation is advantageous in general, because of protection of the contacts, including gates, from air ambient. The application of the second dielectric layer over the gate of AlGaN/GaN HFETs, in turn, often results in an increase of the gate leakage current, which can be explained as a consequence of the strain experienced by the gate. In this work changes in fabrication process flow and a number of AlGaN/GaN HFETs modifications were tested in order to reduce gate leakage currents associated with the second SiNₓ layer.

EXPERIMENTAL DETAILS

The epitaxial structures GaN:Si/Al_{0.25}GaN/GaN used for the fabrication of transistors were grown in-house on 3-inch diameter 4H semi-insulating SiC substrates by low-pressure metal-organic vapor phase epitaxy. A standard fabrication process employing Ti-based ohmic source and drain contacts and an Ir-based metallization to form the gate Schottky contact was used. The surface of the wafers was passivated with 150 nm of SiNₓ deposited by plasma enhanced chemical vapor deposition (PECVD) at 345°C. Gates with 0.5 µm length were defined by optical lithography and opened in SiNₓ utilizing inductively coupled plasma (ICP) etching. After metallization the gates were encapsulated by the 2nd SiNₓ layer having thickness of 200 nm. On-wafer isolation was done by N⁺ ion implantation yielding an isolation resistance of $10^{11} - 10^{12}$ Ω/□ at 100 V.

Wafers from the same growth run were used for all variations of the process flow sequence. The gate leakage currents were monitored on special transistors available at the early stages of the process after gate formation.

RESULTS AND DISCUSSION

Two essentially different conditions in terms of strain in the vicinity of the gate finger were realized in our experiment. Both conditions are represented schematically in Fig. 1. Figure 1 (a) shows the second SiNₓ layer, which has parts deposited on three different technological surfaces, i.e. ohmic drain and source contacts, the first SiNₓ layer and the gate metal. Figure 1 (b) shows top SiNₓ layer, which is mainly deposited on the surface of the first SiNₓ layer. It is reasonable to assume that keeping all parameters the same for both situations, i.e. film thicknesses, deposition parameters, lateral and vertical transistor dimensions, the strain distribution in the transistor active region will not be identical for the two versions shown in Fig. 1. The proposed models in literature suggest that induced strain in AlGaN/GaN structures affects the charge balance between
Figure 1. Transistor structures compared in this work:
a) 1st SiNₓ deposited in the channel region only;
b) 1st and 2nd SiNₓ deposited on top of the complete transistor structure.

surface and 2DEG at the interface [4]. These models mainly deal with the passivation of the bare AlGaN surface in the active area of AlGaN/GaN transistor. In a case of encapsulation the calculation of strain distribution similar to the work of Sacconi et al. [4] may provide more detailed understanding of the difference discussed, but the work here is restricted to the experimental evidence of the effect.

Depending on the subsequent processing steps the openings in the first and/or second dielectric layers are required. The openings locally release stress and reduce the resulting strain in the vicinity of the gate electrode. Two-finger 2×125-µm-wide transistors with design variations of SiNₓ openings according to Fig. 1 were included in the layout for the structure a) and compared to the transistors fabricated using structure b).

The SEM images from the different types of fabricated transistors are shown in Fig 2. The types 1-4 are examples of structure shown in Fig. 1 (a). The type 5 represents the structure shown in Fig. 1 (b). Figure 3 shows leakage currents measured for transistors of types 1-5 according to Fig. 2. The results indicate an increase of the gate leakage current by more than 3 orders of magnitude after deposition of SiNₓ on top of the gates on certain device structures. The degree of deterioration strongly depends on the type of transistor. Thus, type 1 transistors have an average gate leakage current 1.3×10⁻³ A/mm with standard deviation of 0.5×10⁻³ A/mm as measured on wafer at pinch-off condition and \( V_{DS} = 10 \) V.

The type 2 transistors differ from type 1 only by ~ 0.8 µm opening etched in SiNₓ on top of the 1.5 µm wide gate head. The opening acts as an artificial crack in the second dielectric layer releasing the stress, which leads to a reduction of gate leakage current. The average gate leakage in this case was measured 1.6×10⁻⁵ A/mm with standard deviation of 2.8×10⁻⁵ A/mm. We explain increased scattering of the data over the wafer by unavoidable alignment shift of a gate head opening and other possible technological imperfections. There is a limited practical use of the type 2 transistors because of unprotected gate head metallization.
However the obtained result is a direct proof of stress related nature of the increased leakage current. Furthermore, it highlights the importance of the openings in SiNx layers. The windows in both dielectric layers should have proper design to release partially or completely the stress in the vicinity of the gate finger.

Following the results obtained on type 2 transistors, the types 3 and 4 were fabricated on the same wafer for cross-comparison. No improvement in terms of gate leakage current was seen for type 3 transistors as compared to type 1, whereas transistors of type 4 have in average decreased gate leakage current of $6.6 \times 10^{-5}$ A/mm with standard deviation of $1.9 \times 10^{-4}$ A/mm. As can be seen from Fig. 2 the type 4 transistors have boundaries of SiN$_x$ 1st and 2nd layers almost perfectly matched to each other. In this design the parts of the 2nd nitride layer deposited on top of non-SiN$_x$ surfaces (metals and semiconductor) are removed. These parts, in our understanding, are the main cause of the extra stress on the drain-source area.

As a corollary of the results discussed above the best design of transistor should have minimum areas of the 2nd SiN$_x$ layer deposited on top of non-SiN$_x$ surfaces, the situation shown in Fig. 1 (b) and type 5 in Fig. 2. Indeed, the gate leakage current for the transistors of type 5 was measured in the range well below $1.0 \times 10^{-7}$ A/mm. The transistors of both types 4 and 5 have acceptable ranges of the gate leakage current, however significantly better uniformity over the wafer was obtained for the type 5.

In our following processes for discrete GaN power transistors and MMICs the layouts and processing sequence were adapted for transistors type 5, which has resulted in the lowest gate leakage current. The measured leakage currents for two-finger 2×125-µm-wide on these wafers are shown in Fig. 4. It should be noted that transistors are having gates with 0.5 µm length on wafers 1-3 and gates with 0.25 µm length on wafers 4-6. As can be seen from Fig. 4 transistors on all wafers have average leakage current in the range below $5.0 \times 10^{-7}$ A/mm, independently on the gate length. The thickness of the second SiN$_x$ layer was kept 200 nm for all wafers shown in Fig. 4.

Our further investigation will focus on the dependence of the gate leakage current on the conditions of deposition of silicon nitride as well as on thickness of the film, since these parameters are expected to have a strong influence on the residual stress in the dielectric film.

CONCLUSIONS

A key understanding of the nature of the increased gate leakage current in AlGaN/GaN HFETs associated with a dielectric film deposited over the gate is achieved in our experiment. This understanding paves the way for technology optimization depending on particular goals of fabrication. It requires an adapted selection of processing sequence and device layout. The variation of the off-state gate leakage current was measured up to four orders of magnitude depending on the design of the transistor. The increase in the off-state gate leakage has nature related to the residual stress in SiN$_x$ deposited on the gate. As a consequence of this understanding, technological improvements of the fabrication process has been presented and correlated to process stability and reproducibility.

ACKNOWLEDGEMENTS

The authors would like to thank colleagues who helped to take the measurements. Additionally, support from the wafer processing department is appreciated.

REFERENCES


**ACRONYMS**
- HFET: Heterojunction Field Effect Transistor
- SEM: Scanning Electron Microscope
- 2DEG: Two-Dimensional Electron Gas
- MMIC: Monolithic Microwave Integrated Circuit