Reliability Qualification Challenges of a pHEMT-HBT Hybrid Process

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Abstract

The purpose of this investigation is to describe the methodology of reliability qualification of a process that includes two types of transistors and the unique aspects of the combination of these technologies in a hybrid process. Special aspects of performing reliability qualification on a complex process are discussed in general. Methodology of process qualification and some unique findings are described.

INTRODUCTION

Compound semiconductor reliability qualification involves applying various electrical and environmental stresses to evaluation structures in order to accelerate failure mechanisms. Over the years, the appropriate type of stress has been determined for HBT and pHEMT transistors. But what happens when you combine two types of transistors on the same wafer?

The challenges of evaluating a hybrid transistor GaAs process are discussed from a planning perspective and in terms of results that were obtained during the process development stages.

This discussion describes the generic steps of process-type reliability qualifications. Special results and modifications to the investigation will be presented in the chronological order that they were discovered.

APPROACH: WAFERS AND PRODUCTS

The BiHEMT process architecture is a hybrid GaAs/InGaP HBT process co-integrated with an optically-defined 0.7 um gate, InGaP etch-stop, pseudomorphic high electron mobility (pHEMT) process. Both enhancement-mode and depletion-mode pHEMT transistors are available. This process offers both power amplifier and RF switch capability, as well as low-noise performance to facilitate multi-purpose circuits. The process features 2 levels of thick global interconnects, 1 level of local interconnect, and is encapsulated in high performance, low-K dielectric constant interlayer enabling tremendous wiring flexibility and packaging simplicity. Precision nichrome resistor, metal-insulator-metal capacitors, p-n diodes for ESD protection and Schottky overlap diodes are also included. [1]

Typically, a full process qualification involves process elements and a lead packaged product. This investigation will focus on the process elements only.

Process reliability qualification requires aging of the process elements by accelerated testing. The elements can most quickly be evaluated by Wafer Scale Reliability (WSR) testing. This report summarizes the results from WSR testing of the BiHEMT process. WSR is a series of comprehensive on-wafer evaluations of structures including the Process Control Monitor (PCM) and a wide array of special structures designed to find and measure the edges of process capability. The whole wafers are aged and measured to verify the robustness of the BiHEMT process elements. All sample wafers were fabricated at TriQuint's Fab, Hillsboro, Oregon.

The following table summarizes the environmental conditions for each reliability stress that is applied to age bare wafers. Details of the 3 stresses follow.

TABLE 1. IDENTIFICATION OF WAFER SCALE RELIABILITY STRESSES.

Stress	Conditions	Test Point 1	Final Test Point
Air Bake	275ºC Ambient Air	0 hrs	168 hrs
Autoclave	121ºC, 100%RH 15 PSI	0 hrs	96 hrs
Temperature Cycle	-40ºC to +125ºC	0 cycles	500 cycles

The wafer bake is done in ambient air to accelerate thermally activated failure mechanisms and the use environment which is open to the atmosphere. A temperature of 275ºC is preferred for maximum acceleration without compromising the interlayer dielectric material. Data is taken at 0 and 168 hours. As a baseline, the conditions of this test were developed to produce a 20% reduction in channel current for a standard MESFET in TriQuint's TQTRx process and the stress represents 100 years of life at 150ºC.

Wafer autoclave follows JEDEC Standard Number 22, Method A102. The purpose of this test is to apply severe conditions of pressure, humidity and temperature that hasten the penetration of moisture into the material. The test is conducted at a condition of 121ºC with 100% relative humidity at two atmospheres. These conditions create a saturated steam environment which will purposely accelerate beyond nominal humidity conditions. Data is taken at 0 and 96 hours.

Temperature cycling of the wafer follows JEDEC Standard Number 22, Method A104, Condition "G". The purpose of this test is to determine the material's resistance to alternating extremes of high and low temperatures. The stress condition cycles at a low temperature of -40ºC to a high temperature of +125ºC with a ten minute dwell time at each extreme. The test points are at 0 and 500 cycles.

The relative stability of various electrical parameters measured at each defined test point demonstrates the reliability of the different elements built on the BiHEMT process. Since the aging tests are intended to represent lifetimes at use conditions, some aging of the test structures is considered normal. Failure criteria are set generally to represent significant degradation that would equate to performance degradation of products during their use.

An alternative to WSR is Wafer Level Reliability (WLR). The method of wafer-level accelerated lifetesting provides an alternative approach for studying device reliability. WLR involves the stressing and testing of individual test structures on the wafer one-by-one, instead of stressing all structures in parallel with the WSR technique. By eliminating the need for the packaged device, we enhance the flexibility, efficiency, and timliness of reliability studies. In wafer form, it becomes possible to shorten the stress cycle by stressing devices at higher temperatures. The wafer form factor allows for the study of individual devices on a single wafer or on multiple devices on entire wafers. Stressing of multiple devices allows the construction of a spatial map of reliability for a given wafer. Without the package, it becomes easier to observe devices under test and do root-cause analysis of the failure mechanism.[2]

Wafer level reliability stresses include thermal, electrical, and mechanical. Thermal stress is accomplished by auxiliary heater resistors placed around the structure of interest. Oftentimes, self-heating of some elements, such as transistors, can augment the local heaters. Electrical stress is simple application of voltage or current to accelerate mechanisms susceptible to those factors. Mechanical stress is achieved by cycling power through auxiliary heaters causing thermal expansion in the structures of interest. Most typically, WLR tests involve thermal aging of transistors, [2] voltage ramping of capacitors,[3] and power cycling of interconnects.[4]

CONCERNS: ASSESSING RELIABILITY RISKS

To ensure coverage of the highest risk aspects of a new process, an analysis of failure mechanisms is necessary. By using an approach similar to a Failure Modes and Effects Analysis (FMEA), the mechanisms are evaluated in terms of frequency of occurrence. Additional aspects, such as stress, element structure, and measurement variables are also considered. The failure mechanism analysis is a critical step in planning for element reliability analyses. Without the failure mechanism analysis the design and use of applicable test structures and aging methods can be overlooked. Examples of some initial concerns for the BiHEMT process are shown in Table 1.

TABLE 2. INITIAL RELIABILITY CONCERNS OF BIHEMT

Mechanism	Stress	Structure	Measure
Via connectivity over and nearby topography of HBT.	WSR Bake & Autoclave, WLR power cycling.	via chains and via scales	via resistance
Thermal budget contact anneals, hillocks Vs low contact resistance, Base punch-through, etc	WSR Bake	Contact TLMs & capacitors	contact resistance & ramp capacitors to breakdown
Roughness of M0 on etched base after previous lift-off layers. Particularly for 500Å Caps.	Voltage	Big capacitors	ramp to breakdown, extrinsic/intrinsic ratio, defect density
Ti/W interconnect resistance, Moisture susceptibility	WSR Bake & Autoclave, WLR power cycling	Via chains and Hot Via Chains	resistance and cycles to failure
HBT **emitter-base-collector leakage**, filaments	DC yield, WSR bake and autoclave	E,B,C combs	leakage, spacing amplification parameters
pHEMT **liftoff filament shorting**, i.e. "cut gates"	DC yield, HTRB, shut off check	FETs, Hot FETs, Jumbo OFFONLY dense FETs	transistor leakage, Igss, reverse bias leakage
M0 overlay contact integrity with gates, ohmics, NiCr i.e. "cutting"	yield, WSR T/C and Bake	Via chains and alternate inside-outside and 2 dimension overlay via chains	resistance
HBT **Mesa Topology** effects on base liftoff layers G, O, NiCr, M0	yield and WLR Ramp data	mesa proximity of gap scaling structures, meanders, combs	leakage
Delamination at metal and dielectric layers	WSR (A/C) transistor manifolds	PSN on M2 delam patterns	visual inspection delamination
Passivation **hermeticity**, moisture susceptibility	bubble test, WSR A/C, biased humidity on products, WSR Bake	combs, bubble test, products	leakage, bubbles, BCB oxidation

NEW ASPECTS AND CONSIDERATIONS

As a result of the failure mechanism risk assessment summarized in Table 1, a new mask set design was needed to evaluate each of the various combinations of transistors and interactions of the process. In order to include all of the transistor and proximity concerns, the maximum size stepper field was needed. The new design incorporated 144 different modules. These modules were laid out in the form of die, so

that the entire tile emulated a typical product wafer, including the nominal die singulation features that are needed for products.

Of particular concern for the BiHEMT process is the unique topology that is needed to stack transistor epitaxial layers so that multiple device types can be interwoven in the product design. (see Figure 1). The affect of the new feature sizes on nearby circuit elements needed to be investigated and layout proximities needed to be evaluated. Many new structures were used to evaluate layout features at the edge of the layout rules and beyond in order to find the capability limits of the process.

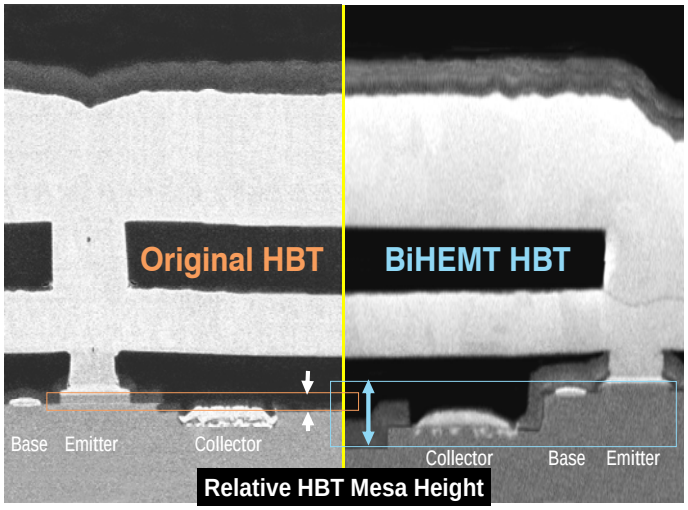

FIGURE 1. THIS IS A SCANNING ELECTRON MICROSCOPE IMAGE OF A FOCUSED ION BEAM CROSS-SECTION SHOWING PHYSICAL DIFFERENCES IN TOPOLOGY BETWEEN STANDARD AND HYBRID PROCESSES. BIHEMT HAS MORE THAN 3X THE TOPOLOGY OF STANDARD HBT STRUCTURES.

For example, huge area mesas (nicknamed as "mountains") were designed in order to exceed the process planarization capability, and then liftoff sensitivity structures were placed at several proximities to the mountains. Figure 2 shows an example of another structure (nicknamed as a "canyon") where the pHEMT device is surrounded by the HBT mesa. The canyon structure was adjusted to determine the worst case proximity of the two transistors and the formation of their associated contact layers. As a part of the wafer design to assess reliability, all combinations of layer proximities were included.

Viability of the physical structures was measured by electrical methods in addition to visual inspections. For example, the formation of metal patterns was evaluated by use of gap structures, comb structures, and meander structures. Separation of the features was monitored by checking for shorting defects over a range of voltages. Since voltage is known to accelerate aging on this style structure, reliability was built into the measurement method. [5]

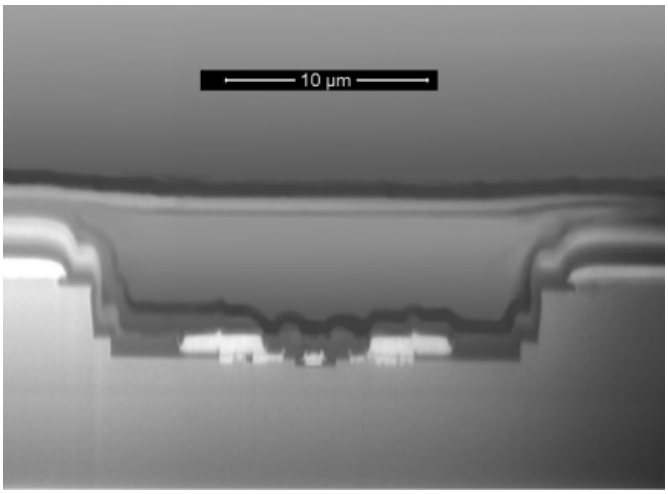

FIGURE 2. AN EXAMPLE OF A "CANYON" STRUCTURE. THIS IS A SEM IMAGE OF A FIB CROSS-SECTION. WHICH SHOWS A PHEMT TRANSISTOR SURROUNDED BY HBT BASE MESA .

In addition to the shorting type defects, continuity defects could also be detected by building daisy chain structures which include multiple contacts or connections. Simple electrical continuity checks at time zero and after the WSR or WLR aging can determine the viability of the physical structures and the influence of topology features in nearby proximity.

RESULTS

Typically, reliability qualification testing is utilized to predict long lifetimes for products utilized under typical conditions. However, reliability investigations during development must first discover any new or life limiting failure mechanisms and then provide clear measurability in order to mitigate those roadblocks. There is nothing better to find these mechanisms and their limitations than a wide array of reliability structures that are intentionally designed to monitor the process capability edges. During the development, where reliability is built into the process, the absolute lifetimes aren't as important as the ability to quickly measure relative reliability. For example, the development team is most interested to find out if the reliability improves or degrades for each new experiment relative to the last baseline. Eventually, the relatively reliability needs to be translated to actual products and to expected lifetimes in use.

In addition to the most early reliability evaluations, the aging aspects are important to establish the capability of a process to perform reliably. Product aspects such as assembly, packaging, and yield need to be included to fully qualify a new process. The ability of WSR relative to other quality and reliability measures was compared during the BiHEMT development. Table 3 shows that Wafer Scale

Reliability stress on reliability structures was able to detect 6 of the eight most concerning failure mechanisms for the BiHEMT process. Two concerns never surfaced. One mechanism not detected by WSR was evoked only by higher volume situations utilizing maximum-sized wafer lots.

TABLE 3. RESULTS: DETECTABILITY OF CONCERNS

Original FMEA Reliability Concern	Development Phase		Manufacturing Integration		
	Product Qual.	PCM Qual.	Yield	WSR Qual.	Product Feedback
Via Connectivity	X	X		X	X
Thermal Budget		X		X	
Met0 Roughness					
TiW Interconnect	X	X		X	X
E-B-C Leakage					
Liftoff			X		X
Met0 Overlay			X		
Mesa Topology				X	
Delamination				X	
Hermeticity				X	X

CONCLUSIONS – BIHEMT RELIABILITY FINDINGS

There were a lot of different results from conducting the qualification evaluations described in this work. In addition to the discoveries on individual tests, the qualification resulted in the following high level outcomes:

1) BiHEMT manufacturing reliability concern identification – a twist on traditional FMEA. Initial failure mechanism risk assessments were found to be accurate through process development, qualification and customer feedback stages.

2) Original BiHEMT development reliability results identified areas needing improvement. Through the WSR method, these outcomes were fast enough to allow improvements, such as modifications to layout rules, even before product designs were completed.

3) Top new aspects of the BiHEMT process (reliability- wise) were found to be: topography, topography, and topography. (see Figure 1 and Figure 2)

4) Wafer Scale Reliability qualification is incredibly fast. In this example: 24 days to complete WSR on three lots.

5) Quick turn qualification using WSR and the appropriate reliability mask set proved to be valuable tools when used as early as possible in the new process introduction process.

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KEYWORDS: reliability, qualification, hybrid, structure, stress, aging, accelerated, wafer-scale, wafer-level.

ACRONYMS:

A/C: Autoclave
B: Base
BCB: BenzoCycloButene
C: Collector
E: Emitter
ESD: ElectroStatic Discharge
FIB: Focussed Ion Beam
FMEA: Failure Modes and Effects Analysis
G: Gate
GaAs: Gallium Arsenide
HBT: Heterojunction Bipolar Transistor
InGaP: Indium Gallium Phosphide
JEDEC: Joint Electron Devices Engineering Council
M0: Metal Zero
MESFET: MEtal Semiconductor Field Effect Transistor
NiCr: Nickel Chromium (nichrome)
O: Ohmic
PCM: Process Control Monitor
pHEMT: psuedomorphic High Electron Mobility Transistor
PSI: Pounds per Square Inch
RH: Relative Humidity
SEM: Scanning Electron Microscope
T/C: Temperature Cycling
TiW: Titanium Tungsten
TLM: Transmission Line Monitor
WLR: Wafer Level Reliability
WSR: Wafer Scale Reliability