Successful Transfer of 12V pHEMT Technology

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Abstract
This extended abstract describes the process that was followed and the results in transferring a 12V pHEMT technology from Freescale Semiconductor to WIN Semiconductors. The process transfer project was divided into four sections: the transfer mask, the epitaxial substrate, the frontside process, and the backside process. To evaluate the success of the transferred process, DC and RF characteristics were measured. In addition, reliability tests were used for the qualification. All success criteria were met.

BACKGROUND
In the early part of year 2000, Freescale Semiconductor (as Motorola Semiconductor Product Sector) developed a GaAs pHEMT technology for wireless infrastructure applications [1]. Freescale continues to develop and support power amplifiers for the wireless infrastructure market including GaAs linear amplifier ICs and discrete power transistors. The high linearity 12 V pHEMT technology, capable of 40V drain breakdown, is a critical part of Freescale RF Division’s amplifier product line. The technology was developed and optimized in the Freescale internal fab over several years.

At the end of year 2008, Freescale closed its GaAs fab commensurate with selling its handset power amplifier business. Since Freescale exited GaAs wafer manufacturing, WIN Semiconductors has been the foundry partner for GaAs wafer manufacturing. A power pHEMT device technology was not part of WIN Semiconductors’ portfolio, and a transfer was necessary to continue the Freescale product line and future development. The goal of the transfer was to produce “drop-in” replacement performance, matching both RF and DC characteristics to the original product.

TRANSFER METHODOLOGY

A joint team with Freescale and WIN Semiconductors engineers was formed at the beginning of the project. The team was made up of product, device, design, test, and fab engineers so that all aspects of the technology and product transfer could be thoroughly explored. By including all disciplines from the beginning, most questions and risks were identified and could be addressed in the development phase. The overall methodology was to use a “copy smart” transfer. After a detailed review of the Freescale process, the team was able to determine what processes could use released manufacturing processes in the receiving fab. By using existing processes at the foundry, the transfer would require less development time, reduce the cost, and go into manufacturing easier.

A key component through the entire transfer process was documentation. The transfer project followed a detailed technology transfer plan and checklist. This included the following key items: schedule, definition of technology and product specifications, process flow information and specifications, risk analysis/FMEA’s, control plans, test data analysis requirements, reliability testing requirements, and product level qualification. Both Freescale and WIN Semiconductors shared the responsibility for documentation items. In addition, all experiments were documented, both short flow and full flow lots included. These results were regularly communicated with the team. The status of experiments running in the foundry was tracked closely so that follow-on activities were ready for completed wafers. With consistent communication, the transfer process ran smoothly.

The transfer process development was divided into four main sections: the transfer mask, the epitaxial substrate, the frontside process, and the backside process.

TRANSFER MASK

The first order of technology transfer is to define a test vehicle that both parties can use to gauge the progress of the transfer. A pizza mask set was created which contained designated test vehicles, such as a product die, reliability devices, PCM test structures and RF-probe-able devices designed from both companies. Involved in this, preliminary design rules were established based on the foundry processes. Probe cards and test codes were also exchanged and reference wafers were tested by both parties to calibrate the
testers. This foundation set the stage for the engineering lots to start.

**EPITAXIAL SUBSTRATE**

One of the critical components of the technology is the epitaxial (epi) material. The epi structure was developed and customized for the application [1]. As part of the transfer, the structure was manufactured by two vendors and evaluated. Wafers from the two vendors and from Freescale epi inventory were included in several of the engineering lots. DC, small signal and large signal RF characteristics were compared. One of the critical parameters, the carrier doping, was calibrated to obtain I-V characteristics matched to the historical data base, such as Imax, Idss, Vth, on-resistance and drain breakdown voltage, etc. Initial data indicated that the on-resistance was off by almost 2x. After thorough discussion with the epi vendor, a revised growth recipe was implemented and brought this parameter to within the control limits.

**FRONTSIDE PROCESS**

The device construction used typical manufacturing methods in the Freescale fab consistent with the equipment set available. In most cases, the process modules were similar to the foundry capabilities and foundry processes were used directly. This was not the case for all modules, particularly the gate module. The original gate process utilized an etched gate channel architecture while the standard foundry gate was formed by evaporation and lift-off. In the course of the evaluation, a single layer liftoff was proved to be inadequate, and a double layer liftoff process was implemented. The layout of the lift-off gate was also changed because the standard metal 1 layer was not combined with gate metal as in the original process. Fig.1 compares the cross sections of gate electrodes from both parties. The difference is obvious and drastic. The rest of the process flow was evaluated throughout the project as electrical performance was measured. Short flow test wafers were used to evaluate individual modules. Once a process was proven capable, full-flow, device-ready wafers were run. The flow was frozen after all electrical performance targets were achieved.

The first layer, ohmic contacts, was formed by electron beam evaporation for source/drain contacts. Device isolation was done by ion implantation followed by the selective first recess etch. The gate was done by bi-layer process for reaching the small undercut with selective recess etch solution. The gate metals, Ti/Pt/Au, was deposited for D-mode pHEMT. Fig. 1 (top) shows the SEM cross-section of single-gate device. After the gate metallization, the pHEMT was fully passivated by SiN, and followed by TaN resistor with sheet resistance 50 ohms/square. Two interconnection metal levels and 200 nm SiN were used for 300 pF/mm2 MIM capacitor. The final protect nitride were adopted for reliability concern.

![Figure 1: SEM cross sections of single gate device. Top image is foundry process and bottom image is original process](image)

**BACKSIDE PROCESS**

There are two packaging lines utilized for this technology, therefore two different backside process flows were required to be transferred. The air-cavity products utilize AuSn die attach using very thin die thickness. The plastic products utilize soft solder die attach with 3 mil die thickness. Process development was required at the foundry for both backmetal schemes. For the AuSn die attach, die thickness had to be evaluated along with backmetal Au thickness to minimize warpage after demount while maintaining sufficient material for die attach. In the final process, the substrate is thinned down to 50 µm and through-via holes are formed by ICP etch. A 6 µm thick Au film is plated as the backside metallization. For the soft solder die attach, the foundry had to develop new processes for the metal layers required, as referenced [2]. Once the process was developed, mechanical sample die were assembled in packages for evaluation. The AuSn die attach quality was...
measured with SEM cross sections and CSAM. A typical CSAM image of a good die attach is shown in Fig. 2.

The soft solder die attach quality was measured with CSAM and cross sections looking for solder attack of the Au backmetal. An optical cross section image of good die attach showing both the source via and backstreet edge is shown in Fig. 3.

EVALUATION AND RESULTS

The first aspect of matching electrical performance was to correlate the test methods. PCM structures, test hardware, and test library algorithms were copied exactly into WIN’s test framework. Freescale and WIN engineering wafers were measured using both test frameworks for comparison. The optimal solution was achieved by combining WIN test structures and test hardware with Freescale library algorithms. Once the PCM test capability was achieved, engineering lots were tested both on-wafer and with packaged product to compare results. The next step was to introduce on-wafer product testing (unit probe). A similar approach was utilized combining Freescale test plans with WIN unit probe framework, and achieved good correlation to product historical performance.

The final process solution provided matching PCM, unit probe, and RF performance. The DC and RF characteristics comparison is shown in Table 1. Figure 4 compares the on-wafer S-parameters of a single unit cell at 12V and a 10%I\textsubscript{diss} bias over a frequency range of 800MHz-15.5GHz. Packaged 10W discrete transistors were measured in fixture using fixed matching conditions at 3.55GHz under the same W-CDMA modulation conditions. Figure 5 compares the gain and W-CDMA ACPR versus output power for V\textsubscript{ds}=12V and I\textsubscript{diss}=140mA for the packaged 10W discrete. The comparison shows that the transferred WIN process maintains the expected 10dB gain level and >30dBm RF power out capability at an ACPR spec of -40dBc. The back-off ACPR characteristic for the transferred process from -40dBc to -44dBc is within an acceptable 1.5 to 2dB level. An automatic load pull system was utilized to compare RF CW performance at drop-in load and source matching conditions which match the W-CDMA product test fixture. RF CW gain and drain efficiency at 12V and 180mA are compared in Figure 6. The WIN process maintains the >10dB gain level, is within 0.5dB for P\textsubscript{1dB}, and shows higher drain efficiency in comparison to the baseline process from Freescale.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>FSL</th>
<th>WIN</th>
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</thead>
<tbody>
<tr>
<td>Vth (V) (1mA/mm)</td>
<td>-0.83</td>
<td>-0.92</td>
</tr>
<tr>
<td>Bvdo (V)</td>
<td>27.81</td>
<td>41.02</td>
</tr>
<tr>
<td>Bvdo (V) (0.1mA/mm)</td>
<td>24.42</td>
<td>35.03</td>
</tr>
<tr>
<td>Bvso (V)</td>
<td>21.27</td>
<td>25.8</td>
</tr>
<tr>
<td>Ron (Ω)</td>
<td>2.39</td>
<td>2.8</td>
</tr>
<tr>
<td>Idsoff (µA)</td>
<td>0.81</td>
<td>2.13</td>
</tr>
<tr>
<td>Ideality</td>
<td>1.29</td>
<td>1.54</td>
</tr>
<tr>
<td>Barrier Height</td>
<td>0.85</td>
<td>0.84</td>
</tr>
<tr>
<td>Ids (mA) (Sat Current)</td>
<td>202.9</td>
<td>218.21</td>
</tr>
</tbody>
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Table 1: DC and RF characteristics comparison of baseline process from Freescale and transferred process at WIN

**Process Control Monitors (PCM)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FSL</th>
<th>WIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth (V) (1mA/mm)</td>
<td>-0.86</td>
<td>-1.02</td>
</tr>
<tr>
<td>Bvdo (V)</td>
<td>25.2</td>
<td>22.07</td>
</tr>
<tr>
<td>Bvdo (V) (10µA/mm)</td>
<td>0.14</td>
<td>0.19</td>
</tr>
<tr>
<td>Idsoff (µA)</td>
<td>1.83</td>
<td>2.05</td>
</tr>
<tr>
<td>Igss (µA)</td>
<td>0.15</td>
<td>0.19</td>
</tr>
<tr>
<td>Idso (µA)</td>
<td>43.82</td>
<td>23.59</td>
</tr>
</tbody>
</table>

**On Wafer Product Test (Unit Probe)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FSL</th>
<th>WIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vgs (V)</td>
<td>-0.86</td>
<td>-0.98</td>
</tr>
<tr>
<td>Vds (V)</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Ids (mA)</td>
<td>307.29</td>
<td>309.58</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>10.94</td>
<td>10.45</td>
</tr>
<tr>
<td>Eff (%)</td>
<td>27,10</td>
<td>39.18</td>
</tr>
<tr>
<td>ACPR (dB)</td>
<td>44.62</td>
<td>43.59</td>
</tr>
<tr>
<td>IRL (dB)</td>
<td>11.02</td>
<td>11.41</td>
</tr>
<tr>
<td>Idsq (mA)</td>
<td>140.41</td>
<td>139.96</td>
</tr>
<tr>
<td>Igss (µA)</td>
<td>77.83</td>
<td>66.97</td>
</tr>
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</table>

**Product Final Test**

**RELIABILITY**

We conducted chip-level temperature step stress (TSS) and 3-temperature stress testing on the parts fabricated at WIN. The performance was verified to be equivalent to the original product. Fig. 7 shows the cumulative failure distribution from the TSS tests. MTTF is calculated to be 2.1e6 hrs and activation energy is 1.49 eV. These numbers
are comparable to the values obtained previously on the parts manufactured by Freescale [3].

A preliminary product level extrinsic reliability was also carried out to get an early check on the product reliability with the chips assembled in production package. The tests included: THB, HTOL, TC and ESD (HBM, MM, & CDM) per Jedec JESD22 standards. Parts pass 1000 hours of THB and HTOL, 1000 cycles of TC, and match original product ESD classes. Even though the process was still being optimized when tested, the preliminary results demonstrate comparable reliability. Product qualification on parts, from qualification lots with frozen epi design and process and assembled according to the production flow, has been started into full extrinsic reliability testing. The qualification plan includes: HTOL, HTRB, HTGB, DCIOL, MSL3, TC, THB, ESD (HBM, MM, & CDM), and manufacturing mechanical indices. Tests have not been completed at the time of this writing.

CONCLUSIONS

A successful transfer was achieved by Freescale and WIN Semiconductors. The “copy smart” methodology was utilized, which combined the strengths from the original fab with the strengths from the foundry. This significantly reduced the development time and reduced risk in introducing potential manufacturing and reliability issues. Technology transfers are complex and difficult. They can be made easier with combined efforts from both the transferring and receiving team members. Consistent and regular documentation and communication between working engineering teams is particularly effective. Parallel efforts to evaluate multiple aspects of the transfer are beneficial when the time comes to combine the entire process for the final evaluation product. All performance and manufacturing criteria were met and new product development utilizing the transferred process is now under way.

ACKNOWLEDGEMENTS

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REFERENCES


ACRONYMS

pHEMT: Pseudomorphic High Electron Mobility Transistor
FMEA: Failure mode effects analysis
PCM: Process control monitor
ICP: Inductively coupled plasma
SEM: Scanning electron microscope
CSAM: C-Mode Scanning Acoustic Microscopy
WCDMA: Wideband code division multiple access
ACPR: Adjacent channel power ratio
CW: Continuous wave
P1dB: One dB compression point
MTTF: Mean time to failure
THB: Temperature humidity bias
HTOL: High temperature operating life
TC: Temperature cycles
ESD: Electrostatic discharge
HBM: Human body model
MM: Machine model
CDM: Charge distribution model
HTRB: High temperature reverse bias
HTGB: High temperature gate bias
DCIOL: DC intermitting operation life
MSL3: Moisture sensitivity level 3