Implementation of Value Added Kaizens (VAK) in a GaAs Manufacturing Facility

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Abstract
In order to be successful in a modern semiconductor manufacturing facility, identification of all cost opportunities must be discovered. The identification of value and non-value added activities can be quite a daunting affair and without training and the proper tools to use, most companies are not successful in reducing non-value added activities. This paper shares the knowledge gained by implementing a value added kaizen (VAK) approach to discover waste (muda) at TriQuint’s Texas facility. Further, this paper shares the knowledge gained using a structured approach at identifying and eliminating these non-value added activities. This paper presents the application of lean principles methodologies that have resulted in reducing cost opportunities reducing reworks, decrease in cycle time that were associated with the elimination of non-value activities.

INTRODUCTION

Value added Kaizens (VAK) are used to identify opportunities in the manufacturing that are often untapped. Included in these opportunities are administrative, manufacturing, engineering, purchasing, planning, logistics, raw material/finished goods and scheduling to name a few. Using VAK aids in identifying opportunities through data collection of the basics of cycle time or quality, and document the impact on lead time. It is important that the data collected during this phase have attributes that focus on quality, cost, yield or cycle-time.

Using the VAK approach a company can
- Document the actual process
- Show the relationship of process steps
- Identify the location of defects/problems/re-work
- Locate value added and non-value added steps of a process
- Lead to improvement “next steps”
- Communicate information
- Train employees on the process

SEVEN-STEP APPROACH TO VAK

The first part of any endeavor must include understanding business key performance indicators to establish the problem process. Constant investigation must take place asking where are we inefficient, where are there lots of “re-work”, where is there frustration, where are we not taking care of the customer?

VAK is a Seven Step Process with specific deliverables in each step. Preparing to launch a VAK is to first review and to stratify the business data to show which specific area to focus on first.

PREPARATION

1. Establish the Theme
2. Establish the Team
3. Establish the Master Plan
4. Understand the resources required,
5. Establish timescales for each of the step and phase activities.

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STEP ONE: DEFINING THE PHENOMENA

Step one of the process is defining the phenomena. In the VAK approach this includes mapping out the process and identify the problems along the way.

It is important to understand value added (VA), non-value added (NVA), as well as necessary non-value added activities and understanding waste (MUDA).

We defined value added activities that transforms material and processing into a necessary product. This is work that the customers are willing to pay for. On the other hand we define necessary non value activities as legal requirements, and internal controls requirements etc. Work that the customers are not willing to pay for, are non value activities which include items that consume resources but does not contribute directly to the production of materials or products or services.

The team physically walked the process, wrote down the steps, identified the key losses and carried out a value added analysis of each step. This resulted in a current process map with opportunities identified

1. 100% inspections were being conducted at After Develop Inspection (ADI).
2. Visually resist dispense amounts appeared to be different from tool to tool (using the same program).
3. There was a large amount of rework activity occurring in all photolithography and mounting areas, this impacted two factory metrics, cycle time and cost. This was verified by reviewing trend charts. This is a critical step at documenting where the current metrics were. Later process improvements could then be verified.

The results of this phase discovered hundreds of opportunities. Table One: displays a snap shot of a process mapping and realization of some non value added activities

<table>
<thead>
<tr>
<th>STEP</th>
<th>DIRECT/INDIRECT</th>
<th>VALUE ADDED/NON VALUE ADDED</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooler Operation delivered lots to Shaper Module for exposure step</td>
<td>Value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator checked lot box for contamination after annealing gold</td>
<td>Non value added</td>
<td>Every next step in the process is your customer</td>
<td></td>
</tr>
<tr>
<td>Stepper Operator checked wafer quality (VIA)</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Acoustic Box and Transfer</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator checked PEG on prepare for etch</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator checked CD on prepare for etch</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator locked up locations of sensitive relations</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator removed targets from location</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator checked R2R for defects after Green</td>
<td>Non value added</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operator performed wafers flatness test part (Step 1/2)</td>
<td>Non value added</td>
<td>Notice put into place to avoid focusing in stepper</td>
<td></td>
</tr>
</tbody>
</table>

Table One: Process mapping

The team used a simple spreadsheet to prioritize those opportunities using a tool referred to as Impact Cost Ease (ICE) analysis.

STEP TWO: STUDY THE SYSTEM

Verification of None Value
1. Added activity and remove
2. Identify the ideal state process
3. From a practical understanding of the process what do you think can really be achieved?

Inspect Reductions
The low volume and high cost of millimeter wave GaAs wafers has historically required each wafer receive a thorough microscopic inspection after develop. This practice continued even though our equipment and processes improved. The recent ramp in volume has brought the inspection operation under scrutiny as a non value added step. Why should so much time be spent inspecting each wafer when the reject rates were very low? The rework rates at each inspection step were analyzed as a basis for a new sample plan. Factors considered were the ease of detection, criticality of the layer, and availability of automated measurements

Cycle Time Issues
There were multiple events that increased cycle time, one was due to a wafer flatness check that was implemented to address reworks caused by hot spots on the stepper. This was a smaller issue to the much larger issue of particles in the factory. The team quickly discovered wafer cassettes, boxes, and wafer transfer issues as well as other defects incoming to photo were a major source of contamination (this is an ongoing activity).

1. Cassettes and Carriers (Au and black particles)
2. Wafer transfer (Au and black particles)
3. Au and particles on tools
4. Pre-dispenses not turned on all tools

Mount Reworks
One of the major reworks that the team came across on one product line was causing a 15% rework rate, since the inception of the product. Wafers are mounted to carriers before grind, the wafers are ground, demounted and shipped for assembly. It is extremely important that these wafers are ground very uniformly as it impacts electrical parameters.

Resist Reduction
During the initial process mapping, on over 60 resist dispense locations, it was discovered that 24 of these appeared to have different amounts being dispense. The team then measured each resist, with the goal of achieving 5g or less per wafer. A complete list of the resists optimized is shown in the results section in table three.
STEP THREE: DEFINE THE CHALLENGE

1. Establish the real gap in performance.
2. Establish Specific goals that Measurable, Achievable, Realistic and Time Bound (SMART).

In this step the team identified the gaps and addressed the problems that prevented the factory from achieving the ideal state, while eliminating major defects.

Examples of SMART GOAL

1. $1000/wafer cost.
2. 30 Day Cycle Time
3. 1% rework rate

In the case of resist usage, it was clear on the initial process mapping that there was considerable waste occurring in the amount of resist being dispensed. A SMART goal for resist dispense was to achieve less than 5g per wafer on non critical layers.

STEP FOUR DETAILED ANALYSIS

1. Analyze each of the Non Value Added activities.
2. Understand their specific problems
3. Root cause them to understand how they may be resolved
4. Eliminate, Combine, Reduce, Simplify (ECRS)

Inspection Reduction

The end result was a simple table (table two) based upon photo process and layer criticality. The vast majority of inspections were reduced from each wafer requiring a low and high magnification inspection to each wafer a macroscopic, first and last wafers a low magnification, and only one wafer requiring high mag.

<table>
<thead>
<tr>
<th>Process</th>
<th>Macro</th>
<th>Low</th>
<th>High</th>
<th>Exceptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Implants</td>
<td>All</td>
<td>First</td>
<td>One</td>
<td>Contact print layers all wafers low mag</td>
</tr>
<tr>
<td>Interconnects</td>
<td>All</td>
<td>Last</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectrics</td>
<td>All</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bond pads</td>
<td>All</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gates</td>
<td>All</td>
<td>All</td>
<td>One</td>
<td></td>
</tr>
<tr>
<td>New technologies</td>
<td>All</td>
<td>All</td>
<td>First</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Last</td>
<td></td>
</tr>
</tbody>
</table>

Table Two—Inspect Sample Plan

Cycle Time Issues

Incoming contaminated cassettes and boxes - there was no Standard Operating Procedure (SOP) governing this activity, resulting in an out-of-control situation in which dirty boxes and carriers were allowed into the photo area. This had the effect of creating unnecessary reworks, the majority of which were the result of defects on the backsides of the wafers, which caused focus problems on the steppers.

It was also discovered that contamination was being introduced by dirty flat finders.

A SOP, for the flat finders, boxes and cassettes is currently being implemented to our ongoing 5S program for photo. This should result in a reduction of particulate contamination caused by the transfer of particles from cassettes and flat finders to wafers.

Mount Reworks

This was an example of a focused improvement project that identified several components using tools such infinity diagrams, interrelation digraphs and then using World Class Manufacturing (WCM) technique referred to as Focused Improvement (FI).

1. Material: Root cause current silicon carrier as specified did not meet tight requirements for process. Re-Specified and scrapped 80% of carriers.
2. Man: Part of the mount process was manual and large operator variation was discovered (gauge R&R). Implemented a semi-automated system.
3. Method: Mount process including coat/bake sequence was re-ordered
4. Machine: Press pressure was optimized. Specification for operating and PM was created

Resist Reduction

Prior experience (both qualitative and quantitative) indicated that for the size of the wafer and topology that resist volume should be no more than 4g/wafer. To be conservative a 5g/wafer maximum was established.

Each resist dispense was measured and compared and targeted for reduction. The results of the reductions can be seen in table 3

STEP FIVE: SOLUTIONS AND FUTURE STATE

1. Develop the practical working solutions to improve the process. (Based upon the ECRS Ideas)
2. Implement the solutions
3. Confirm the new state (Update the process map)
4. Clarify outstanding issues

Inspection Reductions

The second phase of inspection reductions used a rigorous statistical analysis of rework rates to calculate sample sizes. Additional factors such as lot size were included. This phase was fanned out to areas other than photo.

An improved tracking of the inspected wafers was also implemented. The MES system notifies the inspectors of sample sizes upon lot move in via a pop up window. Inspected wafer identities are then collected on lot move out.
This has been the mode of operation for the past six months without any escapes.

STEP SIX: RESULTS

1. Track performance and benefits to confirm success
2. Track and record the relevant improvements
   a. Time reduction.
   b. NVA Task No. Reduction (effort)
   c. Problems eliminated
   d. Calculate Value Added Impact
   e. $ Savings
   f. Increased flexibility
   g. Improved CSI

Inspection Reduction

As a result of the inspection reduction cycle through the photo process decreased significantly as can be seen in figure one.

![Figure One—Inspection Cycle Time Trend of Typical Lots](image)

Cycle Time Issues

The increased cycle times (see figure Two) due to implementing wafer flatness checks and other items are a result of incoming defects to the photo area, while these checks have not been eliminated, the root causes have been identified and action items assigned.

![Figure Two: Work per hour through Photo](image)

Mount Rework

The result of implementing the focused improvement activity surrounding mount rework issues resulted in a reduction of reworks from 17% to 3%. Further, sustainability has been achieved for the past three months.

Rework Reduction

Resist Reductions resulted in significant cost savings (table three) across the factory and supported the Critical Process Indicator (CPI) for the factory.

![Table Three: Resist Reduction](image)

STEP SEVEN: SUSTAINING

Ensure effective roll out of the New Improved Process.

1. Documentation of procedure
2. Change control and risk management.
3. Education & Training

CONCLUSIONS

The concepts of VAK were applied to our photolithography operation. Many non-value added tasks were identified. Using team problem solving techniques, the root cause of a majority of these non-value added tasks were identified. Separate teams were formed to identify the source of these defects, and to eliminate them. The teams that were formed used VAK techniques in guiding their activities and helping them to intelligently prioritize specific areas in which more detailed analyses were required.

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REFERENCES

[1] Poole, Clive Kaizen Consultancy and Training Services (KCTS)
[2] Yamashina, Hajime from the Department of Precision Engineering, Graduate School of Engineering, Kyoto University

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