High-Speed AlInN/GaN HEMTs on SiC and (111) HR-Si

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Abstract

The AlInN ternary alloy provides a lattice-matchable barrier for GaN –based HEMTs that may help improve device stability and reliability. At the same time, AlInN/GaN 2DEGs are far less subject to surface depletion effects when compared to traditional AlGaN/GaN HEMTs when the barrier thickness is thinned down. In principle, the AlInN/GaN material system thus offers a number of potential manufacturability advantages for the realization of deep submicrometer GaN HEMTs. We review progress achieved in the EPFL/ETHZ collaboration on ultrahigh-speed AlInN/GaN HEMT development, on both low-cost HR-Si substrates as well as on traditional semi-insulating SiC substrates. Both technologies have set record cutoff frequencies for GaN HEMTs in 2010, and at writing time AlInN/GaN HEMTs remain the fastest GaN HEMTs ever made on a Silicon substrate.

INTRODUCTION

Because of their now well-recognized combination of physical properties, GaN-based high electron mobility transistors (HEMTs) remain the focus of intense interest for high-power, wideband, and/or high-temperature applications [1]. The key benefits of the (Al,Ga)N/GaN material system for microwave and mm-wave HEMTs are of course associated with their wide energy gaps and the high 2 DEG-channel charge densities resulting from the spontaneous and piezoelectric polarizations associated with the lattice-mismatch between (Al,Ga)N and GaN. In principle, this combination of characteristics enables rugged high-current drive wideband transistors capable of operating at high voltages and temperatures. However, there is growing evidence that the total strain (that is, the lattice-mismatch and piezoelectric contributions) combine to limit the reliability of conventional AlGaN/GaN HEMTs [2-3]. Furthermore, the need to extend GaN HEMTs to operation at millimeter-wave frequencies requires a favorable channel aspect ratio L_G/d so as to minimize short-channel effects and enable higher cutoff frequencies. Gate recessing approaches can be used to alleviate these short channel effects but they may introduce unintended defects at, and below, the etch surface which could affect the device reliability. Another solution is to grow the barrier layer very thin so that no recessing is required. Unfortunately, AlGaN/GaN two-dimensional electron gases (2DEGs) are subject to surface depletion effects when the top barrier thickness is thinned below 15 nm, as clearly discussed in [1]. Some researchers have combined thin Al-rich AlGaN barriers with various dielectrics to counter surface depletion effects, but this approach still faces the strain-related device reliability questions.

AlInN was proposed by Kuzmík as an alternative lattice-matched barrier for GaN–based HEMTs [4] at a composition of 83% Al. The high-Al-content places the AlInN ally closer to AlN than the AlGaN alloy used in AlGaN/GaN HEMTs. AlN possesses the highest spontaneous polarization in the group III-N materials matrix. So even without piezo-polarization, the channel charge density induced by the difference in spontaneous polarization is larger than typically in the AlGaN/GaN heterostructures. This enables the use of a thinner barrier while obtaining the same carrier density at the interface. The feasibility of ultrathin barrier AlInN/GaN HEMTs was recently verified with the demonstration of transistor operation with ultrathin 3 nm AlInN barriers [5]. Such thin barrier would enable higher frequency aggressively scaled devices with reduced short-channel effects and without the need of gate recess, which could improve the device long term reliability and reduce the process complexity.

Recent results on AlInN-based heterostructures showed promising power performance with output power density of

10 W/mm at 10 GHz [6] and 5.8 W/mm at 35 GHz [7]. AlInN/GaN HEMTs have also been reported to show a remarkable stability by surviving operation at temperatures as high as 1000ºC [8]. In the present work, we discuss the interest of AlInN/GaN HEMTs for high-frequency and low-noise operation, with a particular emphasis on results achieved within the EPFL-ETHZ collaborative work.

EXPERIMENTAL WORK

Device processing generally starts by dry etching a 200 nm isolation mesa in a 150 W Cl_2:CH_4:He:Ar plasma. Ohmic contacts were then formed by Ti/Al/Au (16/64/50 nm) evaporation followed by a two-step rapid thermal annealing (30 s at 800°C, followed by 30 s at 850°C) in N_2/H_2 forming gas. Gate electrodes were defined by 30 kV e-beam lithography in a ZEP/PMGI/ZEP resist trilayer, and Ni/Au T-gates were centered in a 1 µm source/drain space. A 100-nm-thick PECVD SiN passivation film was deposited and patterned (SF_6) for contact pads. Ti/Au was used for the overlay metallization. Finally, the encapsulating SiN dielectric was selectively removed only from the immediate T-gate electrode vicinity by taking advantage of the enhanced reactivity of an HF-based wet etch around the gate metal.

Devices on High-Resistivity Silicon Substrates

Figure 1 shows the *I-V* characteristics of our 80 nm gate HEMT [9] measured over V_{DS} = (0 to 6) V with V_{GS} = (0 to –8) V. A maximum drain current of 1.43 A/mm is obtained at V_{GS} = 0 V, while an excellent pinch-off is achieved: at V_{DS} = 6 V and V_{GS} = –7 V, the residual channel current is 4.6 µA/mm only. The devices show well-behaved characteristics, despite some evidence of short-channel effects, as seen from an increased output conductance at V_{DS} > 5 V and V_{GS} < –4 V. As shown below, devices built on SiC feature even higher current densities. Figure 2 shows the peak extrinsic transconductance of g_M = 415 mS/mm measured at V_{GS} = –4.34 V and V_{DS} = 4.0 V. The gate diode leakage remains below 5 µA/mm at V_G = – 8 V. As also shown in Fig. 2, the devices feature an excellent I_{ON}/I_{OFF} ratio of $>10^6$ at V_{DS} = 4 V, which is indicative of excellent channel confinement as well as of the minimal parasitic conduction through the buffer layers. Indeed, the measured inter-device isolation is of the order of 5×10^{10} Ω/sq.

RF measurements were carried out from DC to 40 GHz with an HP8510C vector network analyzer using a line-reflect-reflect-match (LRRM) calibration with off-wafer impedance standards. Before de-embedding, the HEMT shows f_T = 100 GHz and $f_{MAX(U)}$ = 144 GHz. Pads were de-embedded with on-wafer open/short calibration structures by subtracting the Y_{open} from the measured Y_{HEMT} parameters, and then the Z_{short} from the resulting Z_{HEMT} parameters. Specifically, the extracted pad parasitic capacitances were

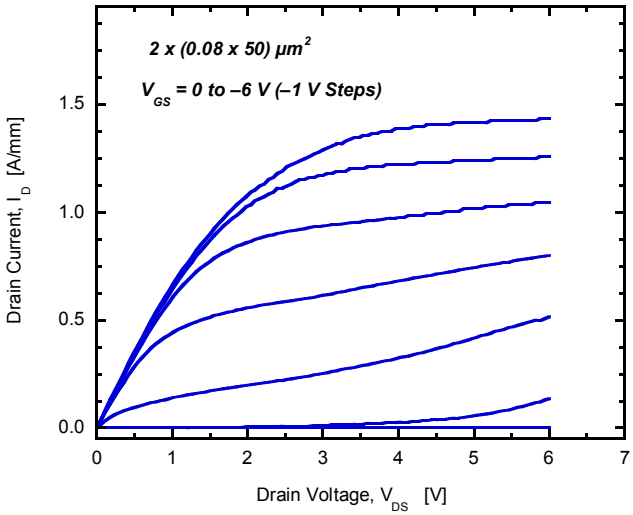

Figure 1. Drain characteristics of 2 × (0.08 × 50) µm² devices measured for V_{GS} = 0 to –6 V, in steps of –1 V [9].

C_{pG} = 15 fF, C_{pD} = 18 fF and C_{pGD} = 1.4 fF (which can be compared to values of 12, 13, and 1.3 fF for similar devices built on semi-insulating SiC). Clearly, the HR-Si substrate and the buffer layers do not represent a serious handicap for the microwave performance of the devices, at least for small-signal operation. Figure 3 shows the resulting transistor microwave performance at the peak f_T bias of V_{DS} = 4 V and V_{GS} = –3.95 V: extrapolation of $|h_{21}|^2$ and of Mason's unilateral gain U with a –20 dB/dec roll-off yields f_T = 143 GHz and $f_{MAX(U)}$ = 176 GHz. Gummel`s method offers an alternative f_T extraction which eliminates some of the uncertainties associated with the usual –20 dB/dec extrapolation from high frequency data [11]: it yields f_T = 142 GHz, in excellent agreement with the usual $|h_{21}|^2$ extrapolation. This f_T value is to be compared with the 205 GHz achieved in 55 nm AlInN/GaN HEMTs grown on SiC [10]. This is by itself a remarkable result in that it shows that AlInN/GaN HEMTs on HR-Si can display similar

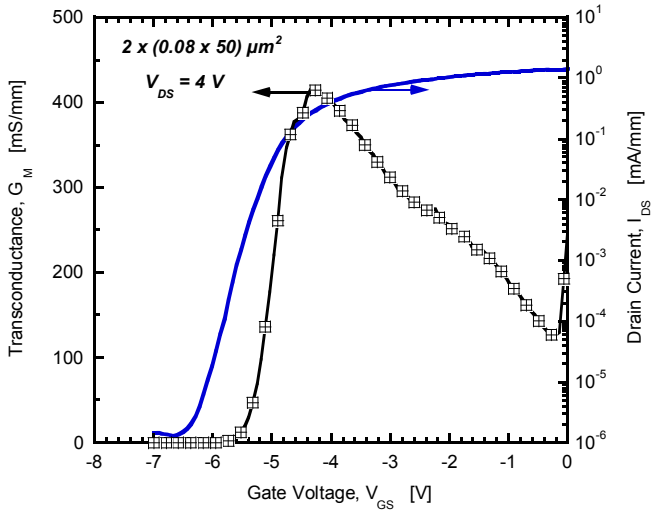

Figure 2. Transconductance and I_D-V_{GS} transfer characteristic for 2 × (0.08 × 50) µm² HEMT measured at V_{DS} = 4 V. The I_{ON}/I_{OFF} ratio is > 10^6 [9].

$f_T \times L_G$ products as devices built on semi-insulating SiC.

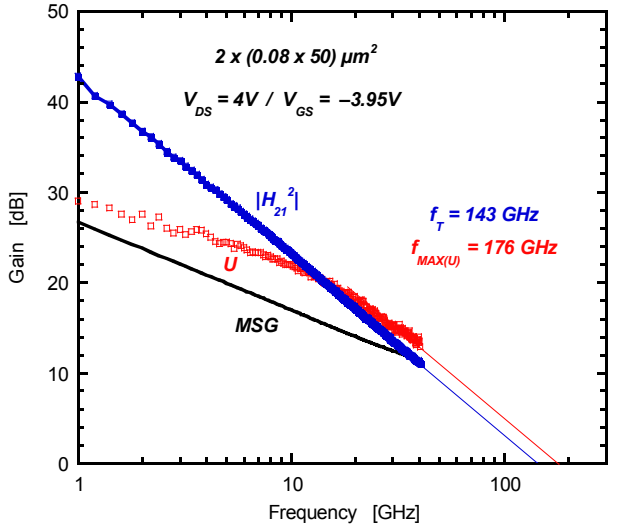

Figure 3. Microwave response for 2 × (0.08 × 50) μm² HEMT on HR-silicon. Extrapolation at –20 dB/dec yields $f_T = 143$ GHz and $f_{MAX(U)} = 176$ GHz at $V_{DS} = 4$ V and $V_{GS} = -3.95$ V [9].

The impact of the dielectric removal immediately surrounding the gate electrode can be gauged by noting that similar devices measured with the full SiN passivation dielectric encapsulation (and thus without measuring the gate footprint) featured a peak $f_T = 130$ GHz with a simultaneous $f_{MAX(U)} = 140$ GHz.

Devices on SiC Substrates

Fig. 4 shows the *I-V* characteristics of our 55 nm gate HEMT measured over $V_{DS} = [0$ to $6]$ V with $V_{GS} = [0$ to $-8]$ V [10]. A maximum drain current of 2.3 A/mm is obtained at $V_{GS} = 0$ V, and a peak extrinsic transconductance of $g_M = 575$ mS/mm is measured at $V_{GS} = -5.3$ V and $V_{DS} = 4.0$ V. The gate leakage is 17 μA/mm at $V_G = -9$ V. The devices show well-behaved characteristics, despite some evidence of short-channel effects as seen from an increased output conductance at $V_{DS} > 4$ V and $V_{GS} < -4$ V.

Fig. 5 characterizes the resulting transistor microwave performance at the peak f_T bias of $V_{DS} = 4$ V and $V_{GS} = -5.3$ V: extrapolation of $|h_{21}|^2$ and of Mason's unilateral gain U with a –20 dB/dec roll-off yields $f_T = 205$ GHz and $f_{MAX(U)} = 191$ GHz. Gummel`s method [11] yields 205 GHz, in agreement with the $|h_{21}|^2$ extrapolation. Fig. 3 shows that f_T and f_{MAX} remain high for a broad range of drain biases, remaining above 160 GHz up to $V_{DS} = 8$ V. Increasing the drain bias to $V_{DS} = 5$ V resulted in a peak $f_{MAX(U)} = 200$ GHz with $f_T = 188$ GHz at $V_{GS} = -5.3$ V. The relatively low f_{MAX}/f_T ratio is caused by the small gate-drain separation (~0.48 μm) used here.

Devices with a larger source-drain distance of 2 μm do show higher f_{MAX}/f_T values [12] compared to identical devices with a 1 μm source-drain gap. The microwave noise properties of such devices were first studied by our group [12]. It was found that despite the relative lack of maturity of AlInN/GaN HEMTs, which is most notably expressed by significantly higher gate leakage currents, they show comparable noise figures to the best AlGaN/GaN devices while offering significantly higher levels of associated gain G_A. The results indicate that the AlInN/GaN system is also potentially extremely interesting for the development of robust low-noise front-ends capable of surviving accidental or aggression-based overvoltage events.

CONCLUSIONS

In the course of the last calendar year, great strides have been taken in the extension of AlInN/GaN HEMTs to higher frequencies on both HR-Si and semi-insulating SiC substrates. In both cases, the results summarized here set records for the fastest GaN–based HEMTs ever built on HR-Si and SiC substrates, and although the absolute record for

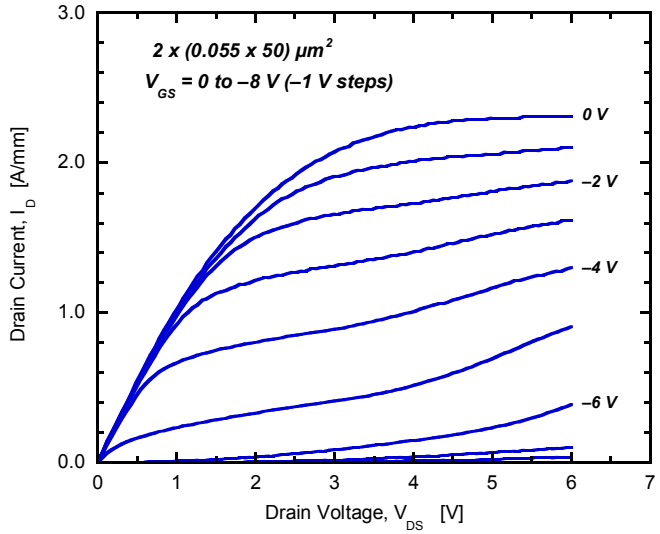

Figure 4. Drain characteristics of 2 × (0.055 × 50) μm² HEMT measured from $V_{GS} = 0$ to –8 V, in steps of –1 V [10].

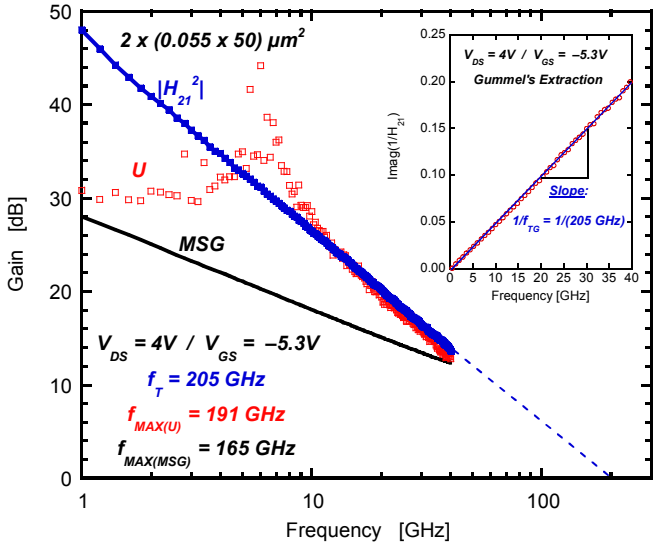

Figure 5. Small-signal frequency response measured at $V_{DS} = 4$ V and $V_{GS} = -5.3$ V [10]. *Inset*: f_T extraction using Gummel's method [11].

speed in GaN HEMTs now returned to AlGaN/GaN devices on SiC, the record on low-cost HR-Si still stands at the time of writing. All things considered, this is a promising evolution for a young material system such as AlInN/GaN HEMTs.

The higher Al–content in the AlInN barriers provide certain clear advantages such as an improved chemical stability that enables devices to stand temperatures as high as 1000ºC and survive [8]. Such feats are clearly beyond the possible realm for conventional AlGaN/GaN devices. However, the higher Al concentration also makes it more difficult to form good Ohmic contacts to the 2 DEG residing at the interface between the AlInN barrier and the GaN channel. This single aspect clearly exemplifies some of the work that remains before us in order to bring AlInN/GaN HEMT technology to the level now enjoyed by more conventional AlGaN/GaN HEMTs.

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ACRONYMS

HEMT: High Electron Mobility Transistor
HR-Si: High-Resistivity Silicon
ICP: Inductively-Coupled Plasma
RIE: Reactive Ion Etching
TLM: Transmission Line Measurement