Improved T-Gate Yield Using E-Beam Trilayer Resist Process

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Abstract

As devices shrink and become harder to produce with the same equipment, decisions must be made to whether it is cheaper to buy new tools or find unique ways to produce smaller and smaller devices. This is especially true for lift-off technologies. As the gate channel shrinks the likelihood of having metal shorts from the metal evaporation increases because the throw distance of the evaporator is not long enough. At TriQuint Texas the evaporation systems have smaller throw distances which create a top and bottom failure on .25um gate bilayer processes with larger gate periphery and consequently yields are not optimal. Investment in new evaporation tools to replace existing tools was in the order of several million dollars. To remain competitive into today's market, investments such as these must be carefully considered and all alternatives explored. As a result of exploring all alternatives, a trilayer resist process utilizing a single developer was developed for the T-gate pattern definition step. The water/IPA mixture of developer was used to accentuate the sensitivity differences between the resist layers, which creates better lift-off profile. We report on the improvement of the dc and final visual yields resulting from this new trilayer resist process.

INTRODUCTION

Larger gate periphery power amplifiers are particularly sensitive to any anomalies in the gate formation process. The metal lift-off process, which is almost universally used in the III-V industry, is especially challenging since it is prone to formation of metal particulates and so-called "stringers". Off-normal directional evaporation effects and insufficient retrograde resist profile can cause increased liftoff-related metal contamination, especially at the edges the wafer. This contamination manifests itself as an increase in dc breakdown failures populated near the tops and bottoms of the wafers. Metal gate channel contamination (GCC) and whisker-like metal strings attached to the gate structure (wings) were found using STEM analysis at the testing failure site. These defects were attributed to the dc failures.

Electron beam lithography was used to define the lift-off gate pattern. With different electron beam energies, the side wall angle from resist profile varies as well. The higher the electron energy, the smaller the side wall angle, which increases the side wall deposition and results in the GCC and wing defects. A third layer of resist was selected and added in the current bilayer process and new developer was used to accentuate sensitivity between resist layers. This trilayer process creates a sufficient effective side wall that eliminates the GCC and wings at the top and bottom of the wafers.

DEFECT INVESTIGATION

Wafer yield map showed DC test failures concentrated on the top and bottom of the wafer as shown in Figure 1. With the aid of the final visual inspection, some defects as shown in Figure 2 were found close to the gate. Further top-down SEM inspection at the top and the bottom of wafers after gate formation was carried out to identify the source of these defects. There were metal strings and particulates found between the source and the drain shown in Figure 3. In particular, they often were located on the side of the gate that is close to the wafer edge. For example, this defect was found on the upper side of the gate where it is at the top of the wafer and on the lower side of the gate where it is at the bottom of the wafer. These and other characteristics of this defect pointed to the evaporation angle as the source of defect. The evaporator systems at TriQuint are characterized by short throw distances that produce an evaporation angle difference of about 2 degrees between the center and the edge of the wafer of a given wafer. The side wall angle of the resist profile from the bilayer resist process at the gate formation step is at 90° ~ 89°. This almost vertical side wall angle is mainly due to the acceleration voltage i.e. 50KeV that was setup in the electron beam lithography tool for production. A STEM analysis was done after the gate metal evaporation before lift-off process. Figure 4 showed metal strings were attached to the one side of the resist side wall. This would explain the metal strings are concentrated on the top and the bottom of the wafer. Therefore, a resist profile with a side wall angle of 88 degree or less is preferred to eliminate this defect.

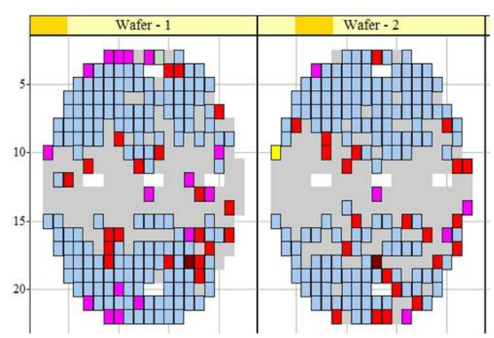


Figure 1 DC failure map indicating top-bottom failure.

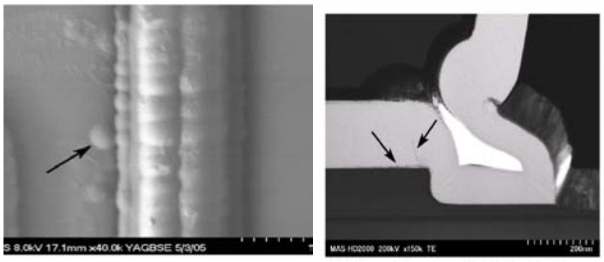


Figure 2 Top view of GCC and wings after SiN dielectric deposition on the left. This defect can be identified at final visual inspection under high magnification. A STEM cross section verified the defect was from gate metal.

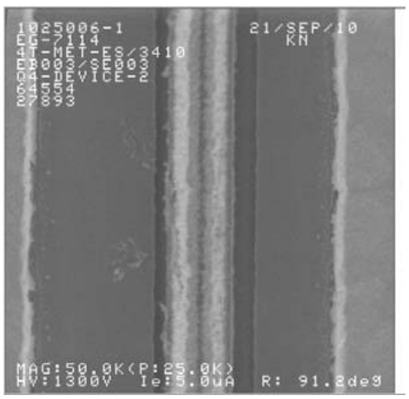
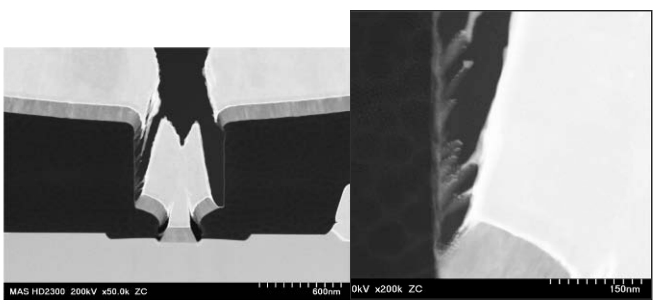


Figure 3 Gate channel contamination (GCC) and whisker-like metal strings (wings) are visible on T-gate after gate metal lift-off process.



(a) (b)

Figure 4 (a) STEM cross section of a bi-layer T-gate before metal lift-off (b) Close-up image of the resist sidewall before liftoff with metal "strings"

PROCESS DEVELOPMENT

Approaches to reduce the side wall angle for better lift-off profile such as using lower acceleration voltage or adding a third layer of resist with lower sensitivity than the second resist layer have been discussed. The former approach will change the shape of electron trajectory near the surface which creates an undercut resist profile [1] and the later one will create a resist overhang. Both will result in reduced side wall angle for better lift-off resist profile. The resist overhang approach was more favorable with the consideration of the exposure conditions of the other processes using the same electron beam lithography tool.

The selection criteria for the 3rd resist were resist profile, compatibility with current processes, and equipment constraints such as develop tank configuration and developer availability. Moreover, the current gate patterning process at TriQuint was a bilayer resist stack, copolymer/PMMA system, exposed with a Hitachi 800D variable shape beam lithography tool. A two-stage develop sequence was used to develop the exposed pattern. The developers were Methanol/IPA mixture followed by the MIBK/IPA mixture. Therefore, PMMA resists with different molecular weight were the ideal candidates [2] to create a resist overhang.

Different developers and develop conditions also have been studied and compared for the sensitivity, contrast, and resolution of the PMMA resist [3, 4, 5]. Based on the selection criteria the resist profiles from the combinations of different trilayer resist stacks and developers were processed and reviewed. Figure 6 showed the resist profile of bilayer and trilayer processes. It showed the effective side wall angle is ~83° for trilayer process.

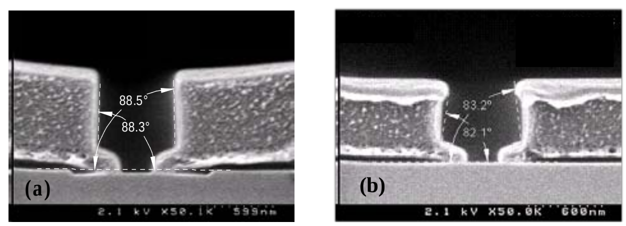


Figure 6 (a) showed bilayer resist profile with a side wall angle of 88.4° (b) showed trilayer resist profile with a side wall angle of 82.5°.

RESULTS AND DISCUSSION

Two test wafers were exposed one with trilayer process and the other with bilayer process. Both wafers processed together through metal evaporation and lift-off process. The gates at the top and the bottom of the wafer were inspected using SEM to document the improvement of trilayer process. As shown in Figure 7 the gates at the top and the bottom of wafer from the trilayer process did not have metal strings and the gates from bilayer process did. A STEM cross section analysis was carried out on the wafers from both processes after the gate metal evaporation before lift-off process. Figure 8 showed the STEM result from trilayer process. It is clear to see that no metal strings attached to the resist side wall on trilayer processed wafers.

Production wafers were split to process on both bilayer and trilayer processes to verify the effect of this side wall angle change. Figure 9 showed wafer maps of DC failures from the process split wafers. The trilayer process did improve the DC yield dramatically.

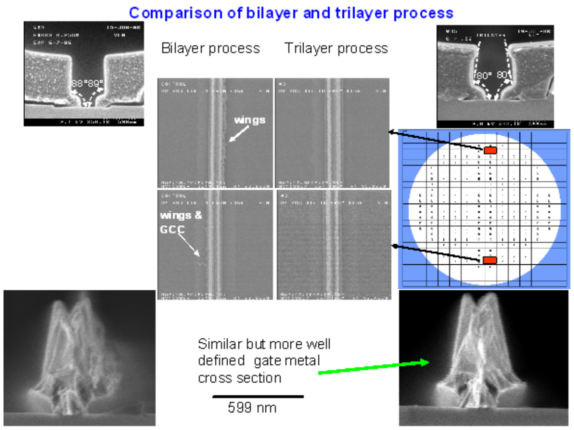


Figure 7 showed the side by side comparison of resist profile, top-down SEM images, and gate metal at top and bottom of the wafer between bilayer process on the left and trilayer process on the right.

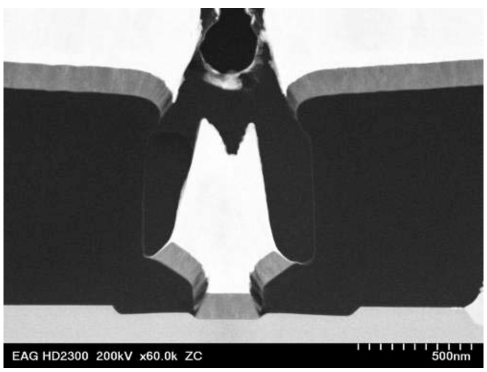


Figure 8 STEM cross section of a T-gate before metal lift-off formed using trilayer resist process.

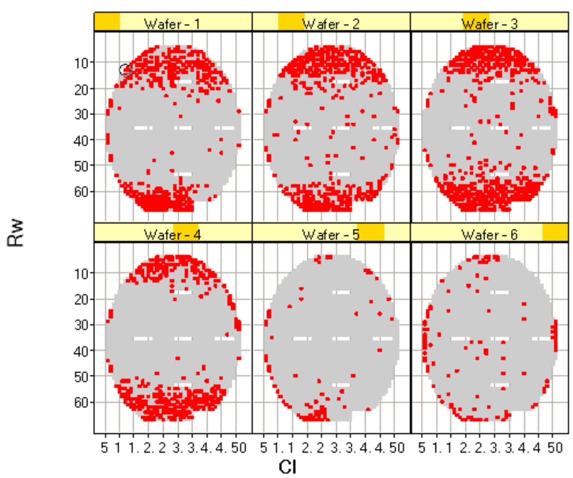


Figure 9 showed the DC failure map of wafers between bilayer process and bilayer process. The gate patterns of wafer 5 & 6 were exposed using trilayer process while the gate patterns for wafer1-4 were using bilayer process.

CONCLUSION

In this study the defect resulting in particular a DC failure type was identified. Through careful observation of the characteristics of this defect the root cause was revealed. Instead of replacing the evaporators which involved capital spending and process qualification, an alternate approach, trilayer process, was developed to prevent side wall deposition at the gate metal evaporation process. A third layer of the resist that is less sensitive to the second layer was selected to create an overhang resist profile which resulted in the effective side wall angle of 83°. This resist profile from the trilayer process successfully eliminated the metal strings and improved DC yields.

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ACRONYMS

GCC: Gate Channel Contamination
STEM: Scanning Transmission Electron Microscope
PMMA: Poly(methyl methacrylate)
MIBK: Methyl isobutyl ketone
IPA: Isopropanol