Development of a Manufacturing Process for Large Diameter Semi-Insulating Silicon Carbide Substrates

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Abstract

Semi-insulating (SI) SiC is presently the substrate of choice for high power AlGaN/GaN HEMTS due to its good thermal conductivity, large diameter and near lattice-match to GaN. During the past several years, II-VI has been developing and improving semi-insulating 6H-SiC substrate manufacturing technology through a joint Air Force Research Laboratory (AFRL) / Missile Defense Agency (MDA) funded initiative. Presently, large-diameter 6H SiC single crystals at II-VI are grown using an Advanced Physical Vapor Transport (PVT) sublimation process. During this effort, substrate diameter was scaled from 75mm to greater than 100mm, while at the same time dramatically improving their crystalline quality and manufacturability. X-ray rocking curve analysis of polished 100mm 6H wafers showed edge-to-edge lattice curvature ($\Delta\Omega$) ~ 0.02° and FWHM of between 14 and 42 arc-seconds. Typical micropipe densities of 100mm 6H material now approach 1 cm^{-2} or below, while dislocation densities of $< 10^4$ cm^{-2} have been demonstrated. Stable semi-insulating properties are readily achieved by compensation with vanadium, which results in highly uniform boule resistivity, on the order of 10^{11} Ohm-cm. Productivity increased by 2.5x and total square inches of commercially shipped substrates increased by a factor of > 3. Manufacturing results will be presented, including defects and yield improvements, material quality, cycle time reduction and process throughput.

INTRODUCTION

DoD's ongoing investment and transition of next generation nitride-based electronics necessitates the availability of affordable, high quality, large diameter SI SiC substrates. A minimum of 100mm diameter substrates are required to leverage existing III-V manufacturing infrastructure and cost efficiencies. Several years ago, Air Force Research Laboratory and Missile Defense Agency partnered to fund an initiative aimed at accelerating the technology readiness of high quality, 100mm SI SiC substrates. Key technical focus areas included crystal growth, fabrication and polishing, cost reduction and manufacturing expansion. This paper summarizes key substrate technology advancements that enabled II-VI to position itself as a leading manufacturer of high quality SiC substrates.

CRYSTAL GROWTH

Traditional crystal growth methods used for III-V semiconductors are not applicable to SiC since it sublimes instead of melting at reasonably attainable pressures. The growth process is based on heating polycrystalline SiC source material between 2000°C and 2300°C under conditions where it sublimes into the vapor phase and subsequently condenses onto a cooler SiC substrate seed [1]. Improving crystalline quality and diameter are highly dependent on the ability to manage a number of key process variables such as controlling hot zone axial/radial thermal gradients, preventing the introduction of unintended impurities or defects arising from the graphite furnace components, maintaining Si/C stoichiometric ratio conditions throughout crystal growth and generation/preparation of high quality seeds.

Significant resources with respect to facilities, equipment and personnel were applied to crystal growth diameter expansion and process optimization aimed at manufacturing very high SI SiC substrates. II-VI relied on a combination of patented Advanced Physical Vapor Transport (APVT) [2] and Axial Gradient Transport (AGT) [3] crystal growth technologies to address the objective of growing large, high quality SI SiC crystals.

Crystal growth is the largest cost center with SiC substrate manufacturing. Manufacturing cost is directly impacted by the crystal growth rate. Slower growth rate leads to increased consumable cost and reduced capacity and growth station throughput. High growth rate can be readily achieved thru an increase in growth temperature, steeper temperature gradients or lower inert gas pressure. However such

an increase can also lead to higher defect density. II-VI developed and implemented strategies aimed at enhancing producibility without impacting quality.
Thermal modeling was instrumental in guiding experimental development in optimizing growth hot zone. Figure 1 highlights a high quality as-grown boule exceeding 100mm in diameter.

Figure 1 As-grown 113.6 mm 6H SI SiC boule.

CRYSTALLINE QUALITY

All relevant material properties were examined using a variety of chemical, structural and electrical techniques. These techniques included AFM, COREMA, Cross Polarizer, Hall Effect, KOH etching, SIMS, X-Ray and Zygo.

Polarized light microscopy is a simple and well established technique used for delineating residual strain around dislocations and other defects [x]. Polished 6H SiC substrates were examined using crossed-polarizer illumination. A low cross-polarizer contrast is a measure of good crystalline quality. Figure 2 compares two crossed-polarizer images of the baseline starting material and current production material. Lack of edge defects are clearly present indicative of a defect-free crystal diameter expansion process.

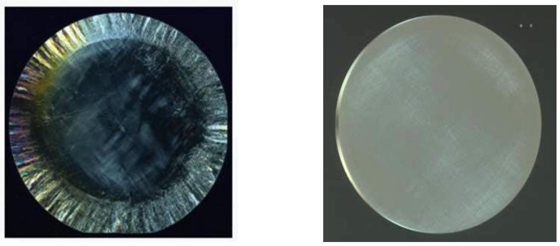

Figure 2 (Left) Cross polarized image of program baseline 100mm 6H SI SiC substrate. (Right) Cross polarized image of typical production 100mm 6H SI SiC substrate.

High resolution x-ray diffractometer (HRXRD) is used for observing the effects of strain and domain mis-orientation (mosaicity) in the crystal. X-ray rocking curve mapping of SiC substrates yields excellent measures of crystalline quality that contain important information on the lattice tilt and sub-grain mis-orientation [4]. X-ray analysis of large-diameter 6H SiC substrates were carried out using a double-crystal Philips 4001 diffractometer. Symmetrical Bragg reflection (0006) was used for evaluation of the substrates with the following parameters: Ω mode, Cu-$K_{\alpha1}$ line and beam size of 1x1 mm^2. Upon scanning across the substrate diameter, the lattice curvature manifests as a smooth variation in the sample angle Ω. The edge-to-edge Ω variation, ΔΩ, is used as a convenient parameter to monitor the lattice curvature of substrates. Early ΔΩ results ranged from 2°-5°. Figure 3 highlights results obtained for a 100mm 6H SI substrate. Typical production edge-to-edge lattice curvature (Δ Ω) is < 0.10° and a full width half maximum (FWHM) of < 40 arc-seconds (KOH etched or polished).

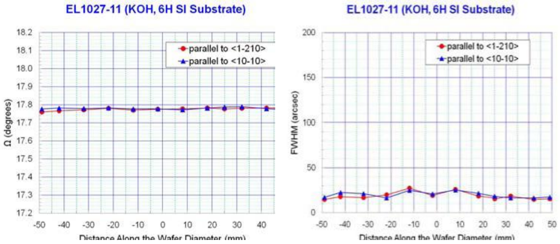

Figure 3 (Right) Edge to edge lattice curvature, (ΔΩ) = 0.02° and (Left) FWHM, 14-27 arc-second, for 100mm 6H SI SiC substrate.

Micropipes are the most widely recognized and deleterious structural defect in SiC. They penetrate the SiC crystal along the *c*-direction and in most cases represent super-screw dislocations with a very large Burgers vector [5]. Micropipe densities (MPD) were measured by etching the wafers in molten KOH followed by automated scanning under an optical microscope. MPD can vary significantly from boule to boule. Any irregularity such as polytype conversion or inclusion could generate clusters of micropipes. In the absence of such growth disturbances, MPD decreases gradually through generations of crystal growth. During the course of the effort, MPD's approaching zero was demonstrated.

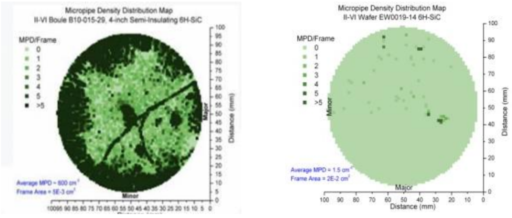

Figure 4 (Left) Micropipe density map of program baseline 6H SI SiC substrate (600 cm^{-2}). (Right) Micropipe density map of typical production 100mm 6H SI SiC substrate (1.5 cm^{-2}).

RESISTIVITY

Semi-insulating SiC substrates are preferred for the fabrication of nitride based RF transistors. Semi-insulating properties can be achieved either by incorporating specific impurities [2] or intrinsic defects [6] into the material to introduce deep energy levels within the bandgap. In both approaches, deep levels compensate for residual shallow donors (N) and acceptors (B) to pin the Fermi level near the middle of the bandgap. II-VI achieves reliable and repeatable compensation with resistivity's reaching 10^{11} Ω·cm by adding precise amounts of vanadium [7] to the growth charge.

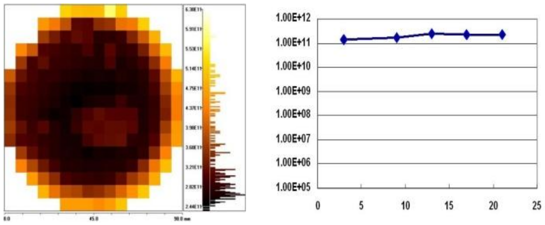

Figure 5 (Left) Corema resistivity map and (Right) axial resistivity of a 100mm 6H SI SiC boule.

Figure 5 illustrates the highly insulating nature of vanadium doped SiC. The electrical resistivity was measured at room temperature using, COREMA, a noncontact capacitance-based instrument. Typical production boules are completely insulating, >E11 Ω·cm, and highly uniform.

FABRICATION AND POLISHING

High crystalline quality, polished 100 mm SiC substrates must satisfy ever changing flatness specifications set by customers. Presently customers are demanding Bow and Warp < 35 um, TTV and LTV < 20 um and 2 um respectively, with no scratches or sub-surface damage. An ultra high removal rate CMP process was developed and optimized in obtaining the best surface finish in terms of local, global and long range roughness and further, without causing defects such as pits and scratches.

The quality of the polished surfaces was measured throughout the effort using AFM and a Zygo optical interferometer.

MANUFACTURING

During the course of this initiative, II-VI invested heavily in facilities and equipment. This included establishment of a new polishing facility in Starkville MS. Key technological innovations associated with growth, fabrication and polishing were fully transitioned into manufacturing. New crystal growth stations were designed with expanded hot zones and automated control electronics to ensure reproducibility. To improve throughput, high-throughput and automated equipment has been implemented, and is currently operational. The use of this equipment will allow reduction of certain current bottleneck process step times by at least 50%.

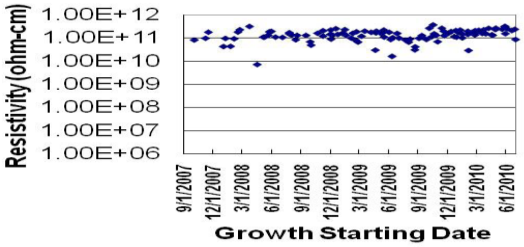

Figure 6 Resistivity Trends of 100mm SI SiC Substrates

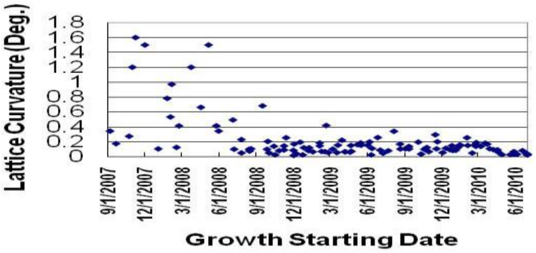

Figure 7 Lattice Curvature Trends of 100mm SI SiC Substrates

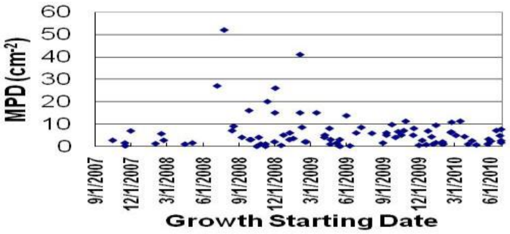

Figure 8 Micropipe Density Trends of 100mm SI SiC Substrates

Figures 6 to 8 show manufacturing trends for resistivity, lattice curvature and micropipe density for a period of nearly three years. The ability to scale production processes while concurrently maintaining high substrate quality is clearly evident.

Figure 9 Productivity improvements.

A key metric II-VI utilizes measures manufacturing throughput of prime wafers/growth furnace/month. This metric considers fabrication and polishing as well. During the course of this initiative productivity improvements have nearly tripled the output of 100mm substrates.

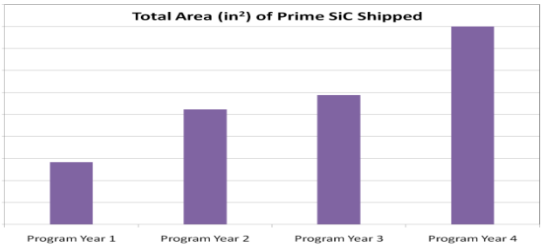

Figure 10 Commercial Sales.

Figure 10 summarizes sales trends during the past four years. Overall sales of SI SiC have increased 3-fold. Demand for 100mm substrates continues to increase as well. This trend is a confirmation that II-VI substrates were able to satisfy ever-changing specifications and performance criteria while concurrently expanding manufacturing capability and reducing cost.

CONCLUSIONS

SI SiC substrates are critical to the manufacture of high power nitride-based RF devices. II-VI has successfully addressed and overcome significant technological challenges to manufacture high quality, 100mm SI SiC substrates. As-grown boule diameter was expanded beyond 100mm. Crossed polarizer's and KOH etching revealed absence of edge defects; validating the reproducibility of the boule diameter expansion process. X-ray rocking curves on 100 mm substrates showed a relatively small lattice curvature with edge-to-edge $\Delta\Omega < 0.1°$. FWHM values ranged between 12 – 40 arc-sec. Typical micropipe density now range 1-3 cm^{-2} for 100mm SI SiC substrates. Reproducible and stable semi-insulating properties with the resistivity reaching 10^{11} $\Omega \cdot cm$ were achieved by doping with vanadium. Manufacturing throughput increased 3-fold. II-VI is now well positioned to respond to future military and commercial requirements for 100mm and larger SI SiC substrates.

ACKNOWLEDGEMENTS

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