6 Inch 0.1µm GaAs pHEMT Technology for E/V Band Application

Hsi-Tsung Lin, Chao-Hong Chen, Shih-Chun Lee, I-Te Cho,
Wen-Kai Wang, and Shinichiro Takatani

WIN Semiconductors Corp. No. 69 Technology 7th Rd, Hwaya Technology Park,
Kuei Shan Hsiang, Tao Yuan Shien, Taiwan (333)
Phone: +886-3-3975999 ext. 1735, e-mail: jameslin@winfoundry.com

Keywords: 0.1µm, GaAs, pHEMT, E band, V band.

Abstract

WIN Semiconductors Corp. has developed a new GaAs pHEMT technology with 0.1µm gate length by using Electron-Beam Lithography and be named as PP10 with the option of 2 mil and 4 mil substrate thickness.

The dc behavior of PP10 illustrates the pinch off voltage of -0.95 V with excellent Idmax of 760mA when gate voltage of 0.5V, which achieve the maximum Transconductance as high as 725mS/mm consequently. The 130GHz of ft with breakdown voltage of 9V exhibits the great high frequency and power performance on this technology.

According to the extraction of MSG (Maximum Stable Gain) from 110 GHz S-parameter measurement, the 8-9 dB gain performance from 70~90 GHz is detected. Additionally, the extremely high power density and the superior performance of noise figure exhibits the potential of integrating E/V band's Tx/Rx core circuit on one chip by using the PP10.

INTRODUCTION

The MMICs with high performance - power density and noise figure - at high frequency will be the key components in next generation wireless infrastructure, and the semiconductor devices will almost dominate the overall performance. WIN Semiconductors Corp. has developed a superior performance 0.1µm GaAs pHEMT technology, PP10. With 130GHz F_t and 180GHz F_{max} aims V/E band PtP radios that provide low cost, easy maintenance, and high data rate of information transference. This technology is produced in 6 inch wafers, high volume of products with high performance, will be used in the backhaul of 3G/4G mobile base station and the radar for airport surveillance.

DEVICE STRUCTURES & PROCESS

The critical dimension of the gate length is defined by Leica direct-write E-beam lithography system and the PMMA/PMAA bi-layer resistance is used for the T-gate shape[1][2], avoiding the gain degradation in ultra high frequency coming from the gate resistance. The high accuracy & resolution properties of E-beam writer are illustratein the Fig.1, which shows a typical PP10 gate with 0.1 µm of foot and 0.5µm top dimension of gate located in only 2µm drain-to-source spacing for achieving ultra low on resistance of channel (see Fig.1).

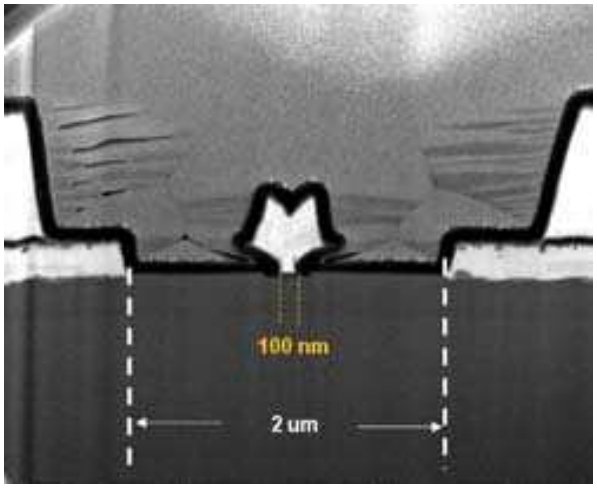

Figure 1. The cross-section piture of the 0.1µm GaAs pHEMT device.

PP10 has been designed with single recess channel geometry to achieve optimum current/transconductance characteristics while maintaining an adequate breakdown voltage for reliable 4V operations. The MMICs are fully passivated using silicon nitride deposited via PECVD and is used as the dielectric for standard 400pF/mm2 Metal-Insulator-Metal (MIM) capacitors.

To provide the product designer additional flexibility, PP10 is available with 100µm or 50µm wafer thickness option. The 50µm substrate thickness provides better thermal management in the package and better confinement of electric fields on microstrip line designs and is especially important for the 60 to 90GHz frequency range. At the same time, the smaller size of backside via available at the 50µm wafer thickness provides a reduction in the gate-to-gate pitch for better signal coherence between each single transistor cell.

ELECTRICAL PERFORMANCE

The dc behavior of typical 2x50µm PP10 device is shown in Fig.2 and Fig.3, the characteristics exhibit the

pinch off voltage of -0.95V with excellent Idmax of 760 mA/mm when gate voltage of 0.5V, which achieve the maximum transconductance as high as 750mS/mm consequently. The knee voltage below a drain voltage of 1V and gate-to-drain breakdown voltage of 9V result in the superior large voltage swing area for the RF signal, and when combined with the high current density, could deliver very high power density.

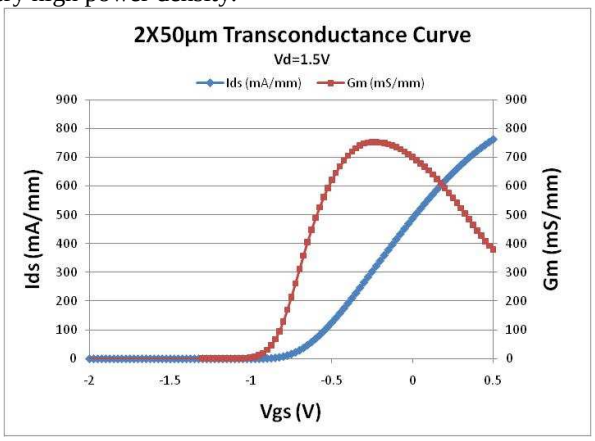

Figure 2. The transcoductance curve of PP10. A high current and trasconductance behavior are observed.

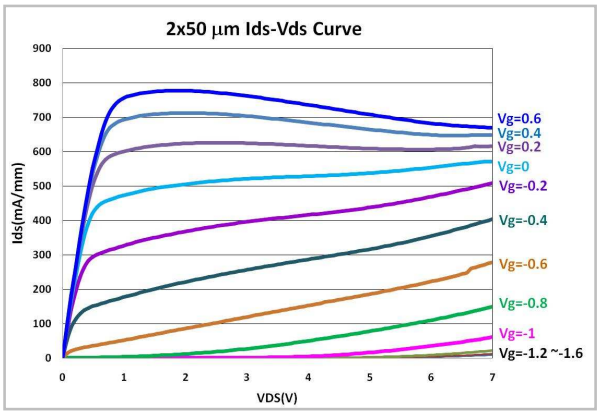

Figure 3. The IV curve of PP10. We can see the knee voltage below a drain voltage of 1V and superior large voltage swing area for the RF signal.

S-parameter measurements taken at V_{ds}= 2V and extraction of Maximum Stable Gain (MSG) to 110GHz is shown in Fig.4 for both 2x25µm and 2x50µm transistors. These data show the PP10 devices provide 8 to 9 dB gain from 70 to 90 GHz.

On the other hand, the extremely high power density of 850mW/mm at 29 GHz on the device of 2x50µm is detected under the drain bias of 4V with the gain and maximum power added efficiency (PAE) of 12dB and 50%, respectively in Fig.5.

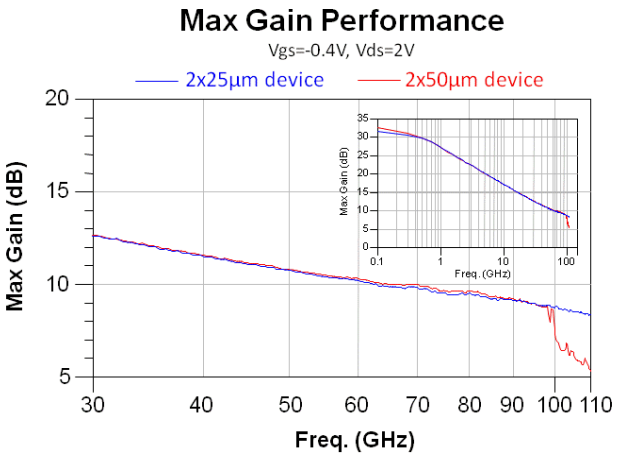

Figure 4. The maximum gain performance is measured by 110GHz S-parameters system. The MSG of both 2x25µm and 2x50µm transistors could be maintained about 8dB at 90GHz.

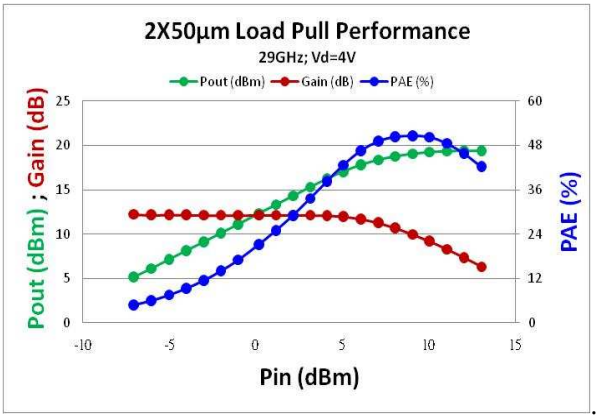

Figure 5. 850mW/mm saturated power density could be reached under 29GHz load pull system, the device is operated at drain bias of 4V.

Fig.6 illustrates F_{min} and associated gain from an 8x25µm PP10 transistor taken at a bias of V_{ds}=2V and 50mA/mm. The excellent noise performance with a minimum noise figure of 0.8 dB and associated gain over 9 dB at 40 GHz is achieved.

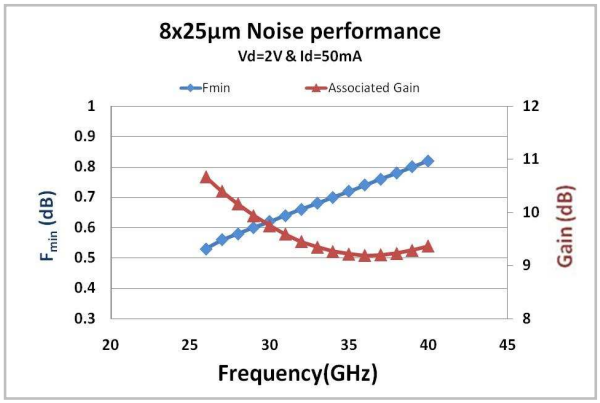

Figure 6. The 26-40GHz noise performance of PP10 that taken at V_{ds}=2V and 50mA/mm.

THE GATE YIELD & UNIFORMITY

Yield of the process is evaluated using FETs with 25 gate fingers and 75um unit width on 150 mm wafers. Yield data is shown in Fig.7. The uniformity of the fundamental transistor characteristics, shown in Fig. 8, is measured using two-gate-finger devices.

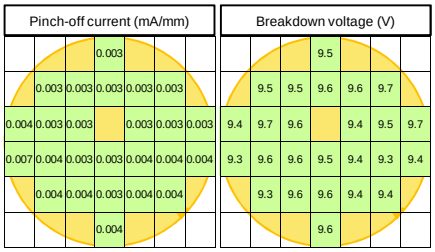

Figure 7. The gate yield is determined by gate leakage, pinch-off, and breakdown performance of the 25×75µm device.

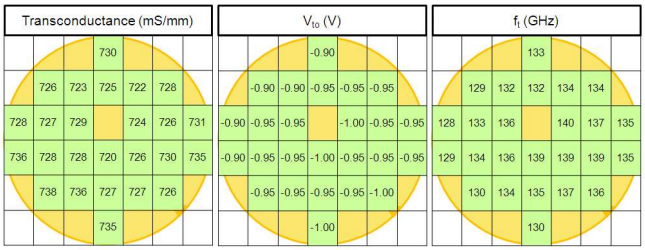

Figure 8. The wafer maps of the key parameters of 2×75µm device show high uniformity.

CONCLUSIONS

The short gate length and the specific design on Epi and process of PP10 result in competitive power and noise performance simultaneously. It allows the product designer to realize a highly integrated multifunctional device with high power amplifier, medium power amplifier and low noise amplifier on one chip for the E-band to V-band Tx/Rx core circuit. With the cost effective 6 inch process capability, the 0.1µm GaAs pHEMT technology could be the right technology for the development of new generation E/V band radio application.

ACKNOWLEDGEMENTS

We would like to appreciate for the support on the 110GHz S-parameter measurement from the Dr. Robin Sloan of Manchester University UK.

REFERENCES

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[2] H.C. Chou, M.C. Liao, et al, "*Design of Experiments to Achieve High Yield Manufacturing at 6-inch Foundry*", GaAs Mantech Conf. April 2002.

ACRONYMS

MMIC: Monolithic microwave integrated circuit.
pHEMT: High electron mobility transistor .
MIM: Metal-Insulator-Metal capacitors.
MSG: Maximum Stable Gain.
PAE: Maximum power added efficiency.