

SESSION 11b: RELIABILITY

Chairs: Peter Ersland, *M/A-COM Technology Solutions*

Chang-Hwang Hua, *WIN Semiconductors Corp*

This year's reliability session includes papers on both active and passive circuit elements, with relevance to both high volume consumer applications, and leading edge high voltage technologies. Our first paper discusses approaches for the reliability qualification of a Bi-HEMT process at TriQuint. Since the failure mechanisms for HBTs and pHEMTs may be quite different, qualifying a technology that incorporates both device types requires careful planning and development of structures to investigate not only each device type individually, but the interaction of these two process technologies on a single wafer. The authors review the wafer scale reliability tests performed, and describe the results of these tests. Our second paper addresses a topic of importance to both reliability and design engineers – thermal performance. A variety of design and process options are investigated by these authors from Skyworks, including different top side metal thicknesses, the location of both through wafer vias and backside thermal vias, and various materials choices. Tradeoffs are described between optimizing thermal performance and minimizing parasitic capacitance for these devices. The third paper in this session describes work performed at WIN Semiconductor to assess the impact of collector design and layout on HBT ruggedness. The authors' results show not only the impact of these factors on Safe Operating Area (SOA), but on device electrical performance as well, and indicate the importance of characterizing SOA on large transistor cells. Our fourth and final paper addresses the effect of layout, dielectric thickness, and the nitride deposition process on capacitor reliability, particularly for use in GaN MMICs. The authors from the University of Ulm and United Monolithic Semiconductors (UMS) present ramped voltage reliability test results that indicate a significant difference in the predicted life time of the three different nitride deposition processes assessed in this study.