Removal of Surface-Related Current Slump in Field-Plate GaAs FETs

F. Hafiz, M. Kumeno, T. Tanaka, and K. Horio

Faculty of systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan

In compound semiconductor FETs, slow current transients are often observed even if the drain voltage V_D or the gate voltage V_G is changed abruptly [1]. This is called drain lag or gate lag, and it is undesirable for circuit applications. Slow transients indicate that dc and RF current-voltage curves become quite different, resulting in lower RF power available than that expected from dc operation [2]. This is called current slump. These phenomena occur due to surface states and/or bulk traps [1]. Experimentally, the introduction of field plate like Fig.1 is shown to reduce the lags and current slump [2]. However, few simulation studies on field-plate structures have been made, although GaN-based FETs with surface states or bulk traps are studied recently [3,4]. Therefore, in this work, we have made two-dimensional transient simulation of field-plate GaAs MESFETs including surface states, and found that surface-related lags and current slump can be reduced by introducing a field plate [5], and they are completely removed in some cases.

Fig.1 shows a device structure analyzed here. The gate electrode extends onto SiO_2 passivation layer. This is called field plate. The field-plate length L_{FP} and the thickness of SiO_2 layer d are varied as parameters. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of pairs of deep donors and deep acceptors. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities are set from $2.5\text{x}10^{19}$ cm^{-3} ($1.25\text{x}10^{12}$ cm^{-2}) to $6\text{x}10^{19}$ cm^{-3} ($3\text{x}10^{12}$ cm^{-2}). As for their energy levels, we take values as previously used [6].

Fig.2 shows calculated turn-on characteristics with and without a field plate when V_D is lowered from 10 V to V_{Don} and V_G is changed from the threshold voltage V_{th} to 0 V. Here, the surface-state density is $1.25\text{x}10^{12}$ cm^{-2}, and surface states are considered on the entire region between source and gate and between gate and drain. In both cases, the drain current I_D remains low for some periods, and begins to increase slowly, showing gate-lag and current-slump behavior. I_D begins to increase as the deep-acceptor surface states begin to capture holes or emit electrons. For the same V_{Don}, the change of I_D is smaller for the case with a field plate, indicating that the current slump is smaller for the field-plate structure. Without a field plate, a barrier for electrons is formed at the gate-to-drain region during the transients, and hence I_D becomes very low. On the other hand, with a field plate, the potential under the field plate is almost flat and a small barrier is seen between the field plate and the drain, and hence I_D becomes larger, resulting in smaller current slump. From these turn-on curves, we obtain quasi-pulsed current-voltage curves. In Fig.3, we plot by (x) the drain current at $t = 10^{-8}$ s after V_G is switched on. They stay rather lower than the steady-state curves, indicating current-slump behavior. From Fig.3, we can definitively say that the lags and current slump become smaller for the field-plate structure.

Figs.4 and 5 show current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, with L_{FP} or d as a parameter. As L_{FP} becomes long or d becomes thin, the current slump is reduced, because trapping effects are reduced. However, the current slump and drain lag increase for very thin d, where the field plate may act like a gate electrode. Therefore, it is concluded that there is an optimum thickness of SiO_2 layer to minimize surface-state related current slump and drain lag in GaAs FETs.

Next, we calculated a case where relatively large density of surface states ($3\text{x}10^{12}$ cm^{-2}) exist at the drain edge of the gate region. This situation can occur after the stress or due to the degradation. Fig.6 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, with L_{FP} as a parameter where d = 0.1 μm. Here the length of surface-state region is set to 0.4 μm. It is seen that when L_{FP} becomes longer than the length of surface-state region, the drain lag and current slump begin to decrease. However, the gate lag is not so changed with L_{FP}. Fig.7 shows calculated turn-on characteristics when L_{FP} = 1 μm and d is very thin (0.01 μm). Here, V_D is lowered from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. Surprisingly, the lags and current slump are completely removed in this case. The reason is not well understood now. This point will be described in more detail at the conference, together with the SiO_2 thickness d dependence of the characteristics.

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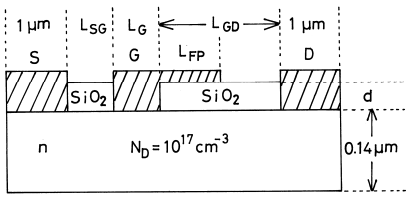

Fig.1 Device structure analyzed here.

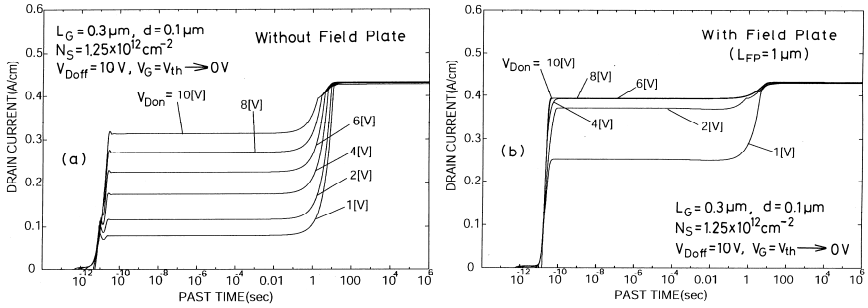

Fig.2.Calculated turn-on characteristics of GaAs MESFETs when V_D is lowered abruptly from 10 V to V_{Don} and V_G is changed from threshold voltage V_{th} to 0 V. N_S = $1.25x10^{12}$ cm^{-2}. d = 0.1 μm. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm).

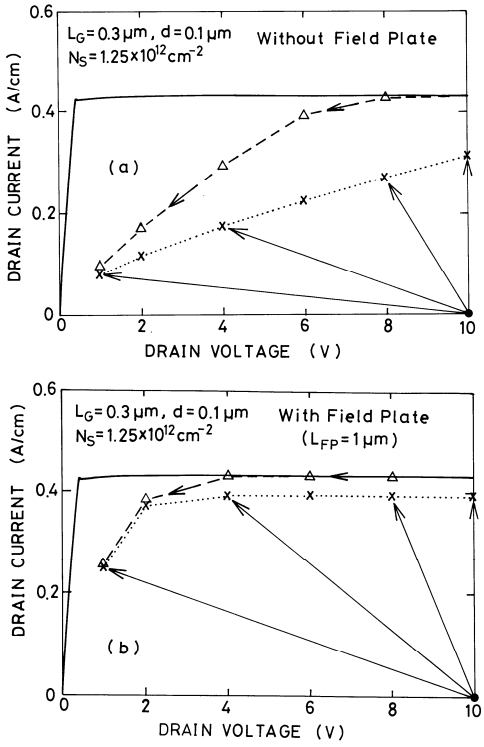

Fig.3. Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (Δ, x) of GaAs MESFETs. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm). (Δ): Only V_D is changed from 10V (t = 10^{-8} s), (x): V_D is lowered from 10 V and V_G is switched on from V_{th} to 0 V (t = 10^{-8} s).

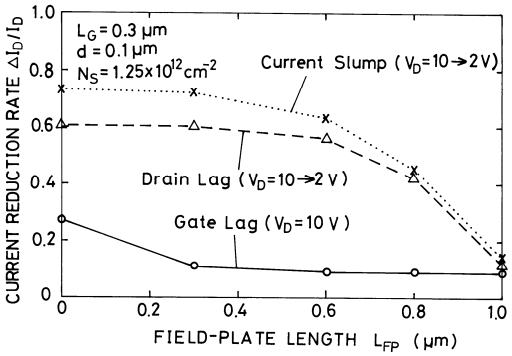

Fig.4. Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. d = 0.1 μm.

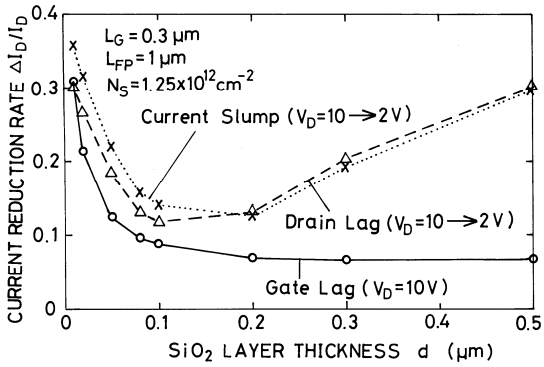

Fig.5. Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with SiO_2 layer thickness d as a parameter. L_{FP} = 1 μm.

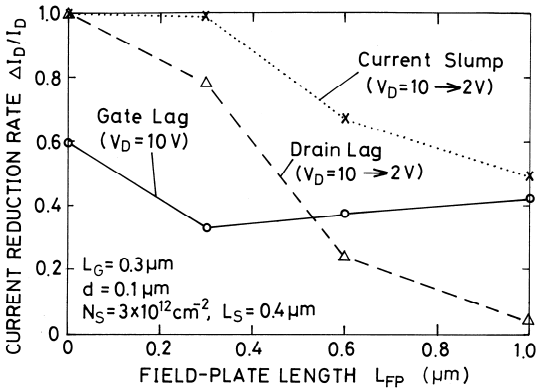

Fig.6. Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. d = 0.1 μm. N_S = $3x10^{12}$ cm^{-2} and the surface-state length is 0.4 μm.

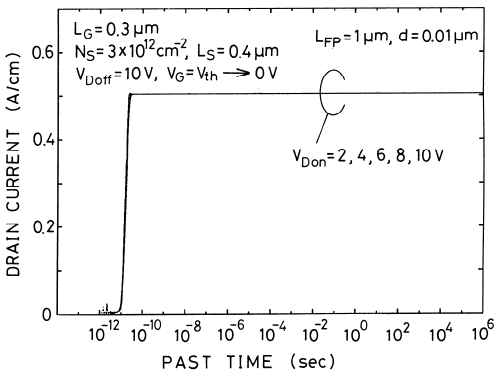

Fig.7. Calculated turn-on characteristics for L_{FP} = 1 μm and d = 0.01 μm when V_D is lowered abruptly from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. N_S = $3x10^{12}$ cm^{-2} and the surface-state length is 0.4 μm.