11.72 cm^2 SiC Wafer-scale Interconnected 64 kA PiN Diode

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To meet the large current handling requirements of modern power conditioning systems, large area devices are required. Presently, material and processing defects set an upper limit on SiC device area that can be fabricated at good yields. Typically, a large number of discrete devices need to be paralleled which increases cost and complexity through dicing, soldering, and forming multiple wire bonds. The latter introduce stray inductance, while high-voltage operation dictates large "keep-out" distances between devices that increase package volume/weight and reduce power density.

The wafer-scale interconnection method first involves the design and fabrication of an array of diodes on a three inch SiC wafer. Based on defect distributions, a diode active area of 0.087 cm^2 was chosen as the optimal size for maximizing area and yield. Diodes are fabricated on 4H-SiC n+ substrates with a 20 µm epitaxial n- drift layer doped to 5 x 10^{14} cm^{-3}. A single implant junction termination extension provides edge termination for each diode in order to maximize breakdown voltage. An initial breakdown voltage test is performed following anode metallization. Devices are selected for interconnection based on limits set for threshold voltage at a leakage current density of 0.2 mA/cm^2. The wafer map of breakdown voltage is shown in Figure 1; a yield of 83% is achieved. The diodes selected all demonstrate a sharp onset of breakdown voltage which is illustrated in Figure 2. A dielectric film designed to withstand high-voltage operation is deposited and anode-sized vias are opened to known-good diodes as shown in the cross-section in Figure 3. Diodes that fail breakdown voltage testing are not interconnected and remain inactive under the dielectric also shown in Figure 3. The anodes of passing diodes are interconnected with a final metallization step to form a large area wafer-scale diode.

Successful demonstration of a wafer-scale diode with an active area of 11.72 cm^2 (135 interconnected diodes) is shown in Figure 4 with a schematic of a "hockey puck" package for pulsed testing. On wafer measurements exhibit a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm^2, and confirm successful wafer-scale interconnection as shown in Figure 5. The wafer was packaged and subjected to high power pulsed testing. A pulsed forming network capable of producing a peak current of approximately 96 kA (~6 kA/kV of charge voltage) for a 470 µsec FWHM pulse width was used to test the full wafer diode. Voltage probe contacts extending radially through the package were used to measure the voltage drop. Under pulsed conditions the wafer-scale diode exhibits a forward on voltage of 10.3 V (at dI/dt = 0) and a peak current of 64.3 kA as shown in Figure 6. This corresponds to a peak current density of 5.49 kA/cm^2 and a diode on resistance of 0.13 mΩ. The diode action, a key parameter in pulsed power operation is calculated to be 1.7 MA^2-sec for the wafer-scale diode. Efforts are presently underway to increase breakdown voltage to 6 – 10 kV for wafer-scale interconnected PiN diodes and thyristors. This work is supported by the US Army Tank Automotive Research and Development Engineering Center (TARDEC), under program manager Joe White.

Additional data on high voltage large area interconnected SiC PiN diodes will be presented in the extended abstract.

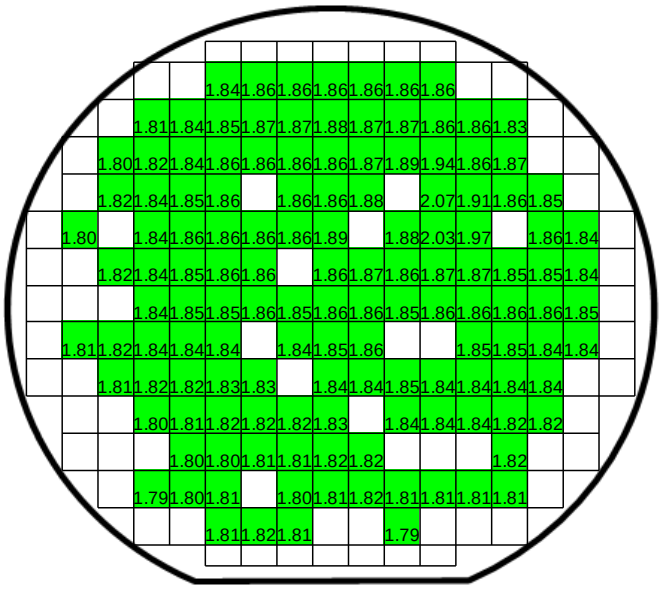


Fig. 1. Wafer map of PiN diode breakdown voltage. The yield is 83% (diodes in green pass) at a leakage current density of 0.2 mA/cm^2.

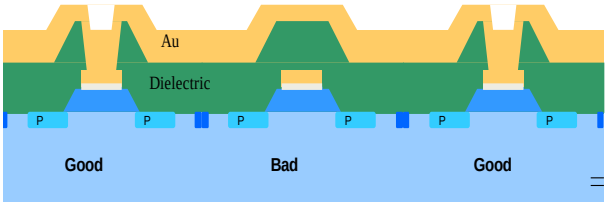


Fig. 3. Anodes of PiN diodes passing breakdown voltage testing are interconnected across the wafer. Diodes that fail breakdown voltage testing are not interconnected and remain inactive under dielectric.

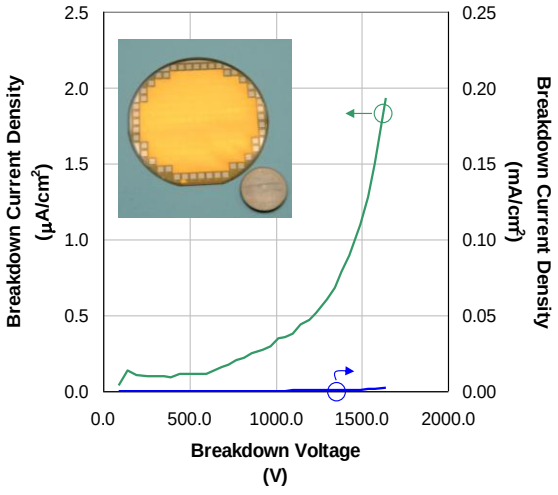


Fig. 5. The wafer-scale interconnected wafer exhibits a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm^2.

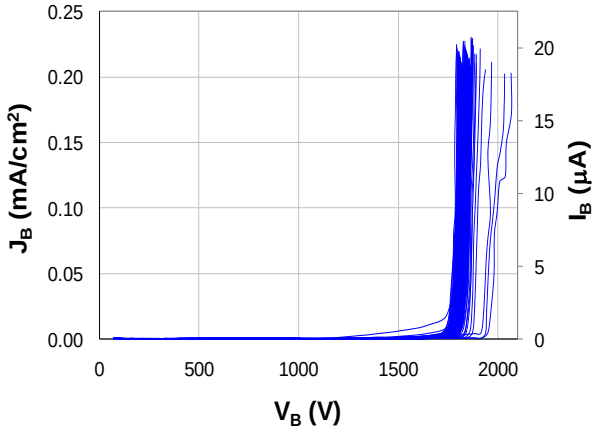
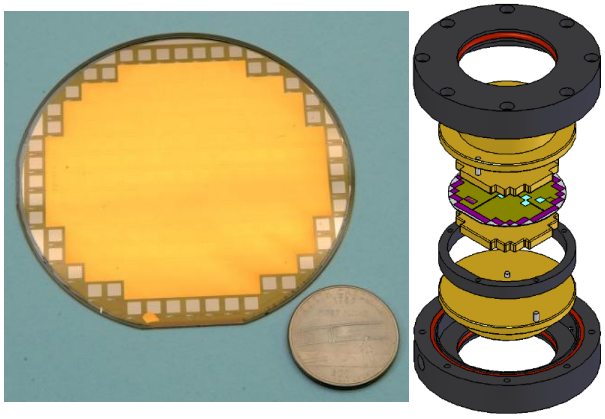


Fig. 2. PiN diodes selected for wafer-scale interconnection demonstrate low leakage currents and sharp onsets of voltage breakdown.



(a) (b)

Fig. 4. Photograph of the wafer-scale interconnected diode. The active area is 11.72 cm^2 (a). Schematic of a "hockey puck" package for pulsed testing (b).

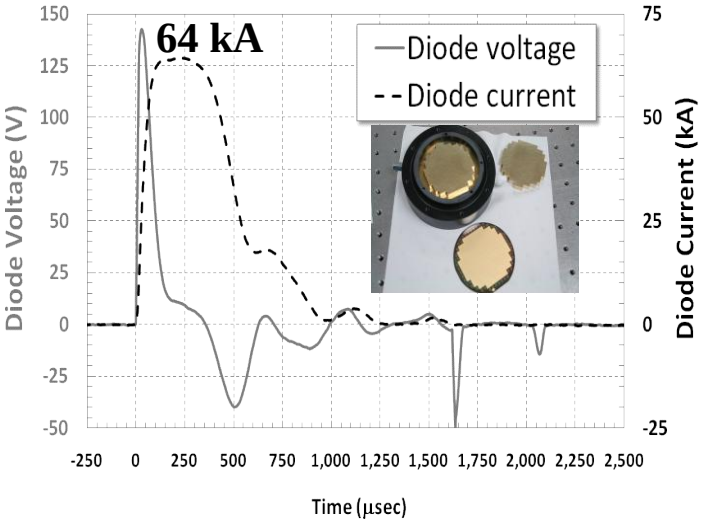


Fig. 6. The 1790 V wafer-scale interconnected diode is pulsed at a peak current of 64.3 kA (5.49 kA/cm^2). The forward on voltage is 10.3 V and the diode action is calculated at 1.7 MA^2-sec.