# Inverted-type InAlAs/InGaAs MOSHEMT with Regrown Source/Drain Exhibiting High Current and Low On-resistance

Qiang Li, Xiuju Zhou, Chak Wah TANG and Kei May Lau*

Department of Electronic and Computer Engineering,
Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong.
Tel: (852) 2358-7049, Email: eekmlau@ust.hk

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**Abstract**

As Si CMOS devices scale into sub-22nm regime, severe short channel effect and power-dissipation constraints lead to huge challenges. To maintain high switching speed while lowering power consumption, high on-current at low supply voltage is required for future generation of novel transistors. III-V high-mobility channel FETs are currently under intensive investigation for such applications and various device architectures have been explored. Inversion-channel InGaAs MOSFETs with $Al_2O_3$ [1], $Al_2O_3$/GGO[2], or $Al_2O_3/Y_2O_3$ [3] as gate dielectric have yielded impressive performance. However, due to the limitation of source/drain dopant activation after ion implantation, the access resistance of these devices is usually large. InAlAs/InGaAs buried channel or quantum-well structure is another attractive candidate because of its superior electron mobility and flexible heterostructure engineering. 30nm gate-length InAlAs/InGaAs HEMT with promising logic figures of merit has been reported [4]. But conventional HEMTs with recessed gates are undesirable for VLSI application due to the large footprint. One emerging alternative device design is incorporating regrown source/drain for ohmic contact, which eliminates gate-recess etching in the meantime. Using this approach, InP/InGaAs composite channel MOSFET on InP substrate with maximum drain current exceeding 1300 mA/mm has been demonstrated [5]. In this work, selectively-regrown source/drain was applied in inverted-type InAlAs/InGaAs MOSHEMTs metamorphically grown on GaAs substrates. Sub-micron gated devices have exhibited drain currents exceeding 1100mA/mm at Vds=0.5V with ultra-low on-resistance.

We developed a gate-last non-self-aligned process for the fabrication of MOSHEMTs with regrown source/drain. $SiO_2$ or $SiO_2$ /$Al_2O_3$ films were first deposited on as-grown HEMTs as regrowth mask, The source/drain regions were exposed by wet etching down to the InGaAs channel layer. Heavily n-doped InGaAs source/drain regions were regrown in a AIXTRON 200/4 MOCVD system, and the regrowth mask was removed by BOE subsequently. Mesa etching was then performed for device isolation. After surface cleaning by 10% diluted HCl and $(NH_4)_2S$ treatment, $Al_2O_3$ was deposited as gate dielectric using atomic layer deposition (ALD). Post deposition annealing (PDA) was conducted to improve the oxide quality, followed by source/drain contact holes opening and metal (Ni/Ge/Au/Ge/Ni/Au) deposition. Ti/Au gate metallization was the final fabrication step. The cross-section view of InGaAs MOSHEMTs after process is depicted in Fig.1 (a). Fig.1(b) shows the AFM image of source-gate-drain surface profile after regrowth and gate oxide deposition. Three samples have been prepared with different $Al_2O_3$/InAlAs thicknesses and PDA conditions, detailed in Table I.

Two transmission line matrix (TLM) patterns have been designed, and the cross sections of them were shown in Fig. 2. Table II summarized the access resistance and intrinsic channel resistance of MOSHEMTs after the gate-last process. The 60nm thick regrown $n^+$-InGaAs showed a sheet resistance (Rs) of 21-22Ω/sq. The contact resistance (Rc) of metal on regrown-InGaAs varied from 8 Ω·μm to 13 Ω·μm. Sample S3 exhibited the smallest regrowth interface resistance (around 0.027 Ω·mm) among them. The output characteristics of the three samples were compared in Fig.3. Sample S1, S2 and S3 exhibited maximum drain current Idss of 599mA/mm, 871mA/mm, 1132mA/mm at a small bias of Vds= 0.5V, respectively. The raised source/drain with high doping level resulted in ultra-small on-resistance, which is 676 Ω·μm, 370Ω·μm and 350Ω·μm for S1, S2, S3 respectively. Fig.4 shows the gate leakage characteristics. Fig.5 gives a comparison of on-current at Vds=0.5V of recently reported high-performance InGaAs transistors. Enhancement-mode MOSFET, HEMT, as well as depletion-mode InGaAs transistors with regrown source/drain are all included. The device reported in this work shows the highest current delivering capability.

**Reference:**

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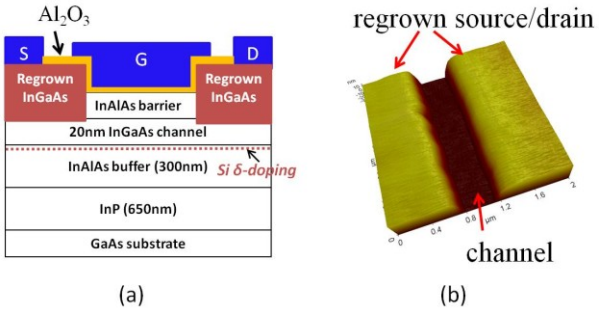


**Fig.1 (a):Cross-section view of InGaAs MOSHEMT; (b):AFM image of source-gate-drain surface profile**

TABLE I

**Structure and process parameters for the samples studied in this work**

| Parameter | Sample S1 | Sample S2 | Sample S3 |
|---|---|---|---|
| InAlAs barrier | 8nm | 12nm | 5nm |
| HEMT sheet resistance by Hall measurement | 300 Ω/square | 308 Ω/square | 330 Ω/square |
| Gate oxide $Al_2O_3$ | 15nm | 8nm | 8nm |
| PDA condition | 530°C in $N_2$ for 30sec | 380°C in forming gas (20% $N_2$) for 30min | 380 °C in $H_2$ for 30min |

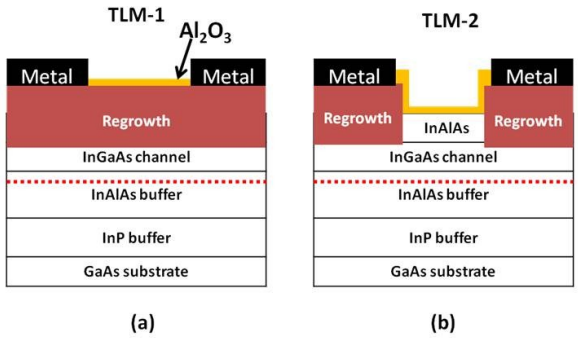


**Fig.2 Cross-section schematic of TLM patterns**

TABLE II

**TLM characterization results after gate-last process**

| Sample | TLM-1 | | TLM-2 | |
|---|---|---|---|---|
| | $R_S$ (Ω/sq) | Rc (Ω·mm) | $R_S$ (Ω/sq) | Rc (Ω·mm) |
| S1 | 21 | 0.013 | 361 | 0.26 |
| S2 | 22 | 0.01 | 525 | 0.35 |
| S3 | 21 | 0.008 | 555 | 0.035 |

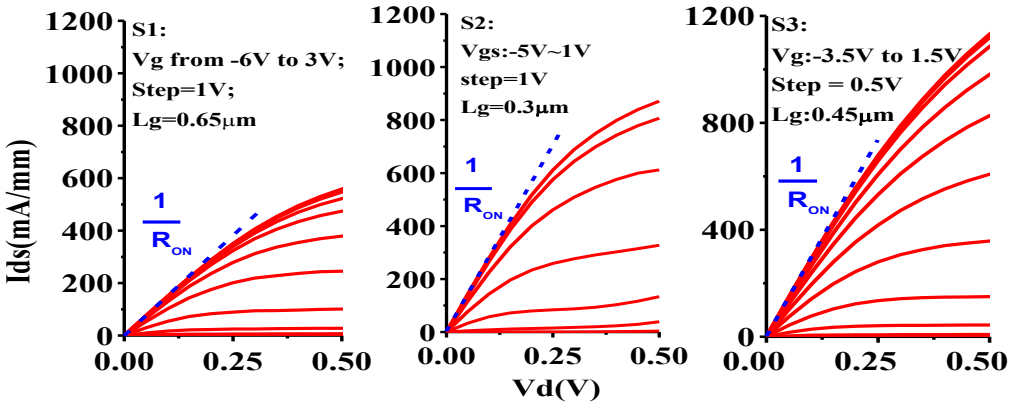


**Fig.3 Output characteristics of Sample S1, S2 and S3.**

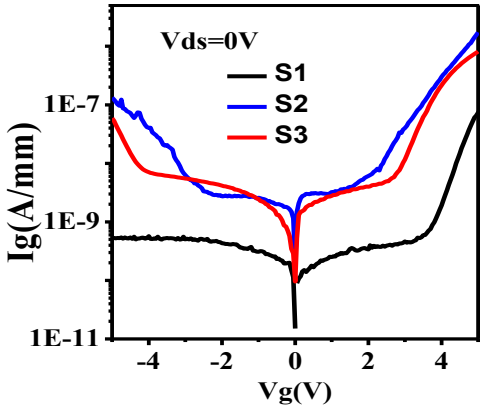


**Fig.4 Gate leakage characteristics**

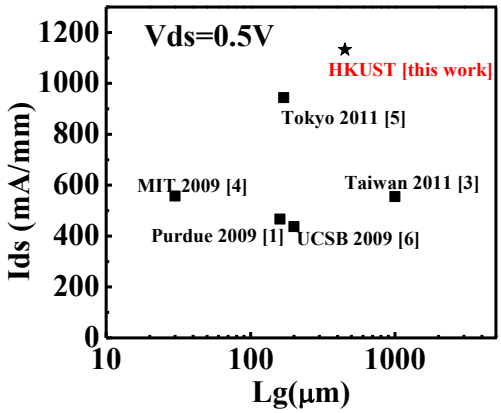


**Fig.5 Comparison of on-current at a drain bias of Vds=0.5V**